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13. ABSTRACT (Maximum 200 words)

A large number of applications for power switching devices lie in the voltage range from 600 – 1800 V. In this regime, the specific on-resistance of SiC power MOSFETs is limited by their MOS channel resistance, due to the low inversion layer electron mobility at the SiO_2/SiC MOS interface. Although significant progress has been made in increasing the electron mobility, it is still about an order-of-magnitude lower than in silicon devices. Our approach to this problem is to implement *structural* changes, namely short channel lengths, that will directly reduce channel resistance *independent of and in addition to* any improvements in channel mobility. The short-channel DMOSFETs utilize a novel self-aligned implantation process that easily and reliably produces sub-half-micron channel lengths. Punchthrough of the short channel is avoided by appropriate tailoring of the channel doping. DMOSFETs have been fabricated on 20 μm (nominal 2 kV) and 50 μm (nominal 5 kV) n-type epilayers on 4H-SiC, and **the on-resistance of these devices is not dominated by MOS channel resistance**. Work on DMOSFETs on 6 μm epilayers (nominal 1 kV devices), and on UMOSFETs, is continuing. This report concentrates on the results on 20 μm- and 50 μm-epilayer DMOSFETs.

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1.INTRODUCTION

1.1 Silicon Carbide (SiC)

Silicon carbide (SiC), first discovered by Jon Jacob Berzelius in 1824 [1] in his attempts to make synthetic diamond, is set to revolutionize the power semiconductor field. Current SiC research is being driven by the growing promise of applications such as: high power/high voltage power switching devices, RF power device, and IC's operating at high temperatures and in high radiation environments. The attractive properties of SiC as a power semiconductor material in comparison to Si and other semiconductor materials are stated below:

1.1.1 SiC: a wide bandgap material

Table 1.1a

Property	4H-SiC	6H-SiC	Si	GaAs
Bandgap Eg(eV)	3.26	3.03	1.12	1.43

The SiC bandgap (4H-SiC, 3.26eV, [2]) is almost 3 times higher than that of Si. Therefore in SiC devices, due to negligible thermally generated electron-hole pairs, leakage current and heat generation problems can be avoided. The high intrinsic temperature (800 °C) also allows SiC power devices to achieve stable operation at high temperatures. Another useful application of this large bandgap ($Eg = h\gamma = hc/\lambda$) is in optoelectronics, where UV photodetectors are able to detect short wavelength light. The large operating temperature range and stable operation also make SiC material extremely suitable for temperature, pressure and UV sensors.

1.1.2 High breakdown electric field

SiC is the semiconductor of choice as power semiconductor devices due to its high critical electric field. The critical electric field (E_c) in SiC is 8 times higher than Si, depending on doping (N_D), and an E_c (V/cm) vs. N_D (cm^{-3}) plot is shown in Fig. 1.1. The critical electric field determines the onset of avalanche breakdown within the device and the following relations are used for Si and 4H-SiC [3], [4], [5]:

$$E_c, Si = \frac{4\times10^5}{1-\frac{1}{3}\log_{10}\left(\frac{N_D}{10^{16}}\right)} \tag{1.1}$$

$$E_c, 4H-SiC = \frac{2.49\times10^6}{1-\frac{1}{4}\log_{10}\left(\frac{N_D}{10^{16}}\right)} \tag{1.2}$$

$$E_c, 4H-SiC(experiment) = (5.2\times10^4)N_D{}^{0.104} \tag{1.3}$$

(Power law expression fitted to experimentally obtained data)

The blocking voltage V_{BR} of a "non-punch through" power MOSFET using 1D analysis is then given as,

$$V_{BR} = \int E(x)dx = \frac{\varepsilon_{sic}E_c^2}{2qN_D} \tag{1.4}$$

where ε_{SiC} is the dielectric constant of SiC (F/cm), and q is the charge (C). V_{BR} varies as the square of the E_c and is thus ($\varepsilon_{SiC}E_{SiC}{}^2/\ \varepsilon_{Si}E_{Si}{}^2$) 60 times higher than in similar Si power devices of the same doping N_D. For a given blocking voltage, SiC devices can use a higher drift layer doping and thinner drift regions than that required for Si devices.

The specific on-resistance $R_{on,sp}$ consisting only the drift layer resistance for a "non-punch-through" design is given as,

$$R_{on,sp} = RA = \rho W_D = \frac{4V_{BR}^2}{\mu_{bulk}\varepsilon_{sic}E_c^3} \tag{1.5}$$

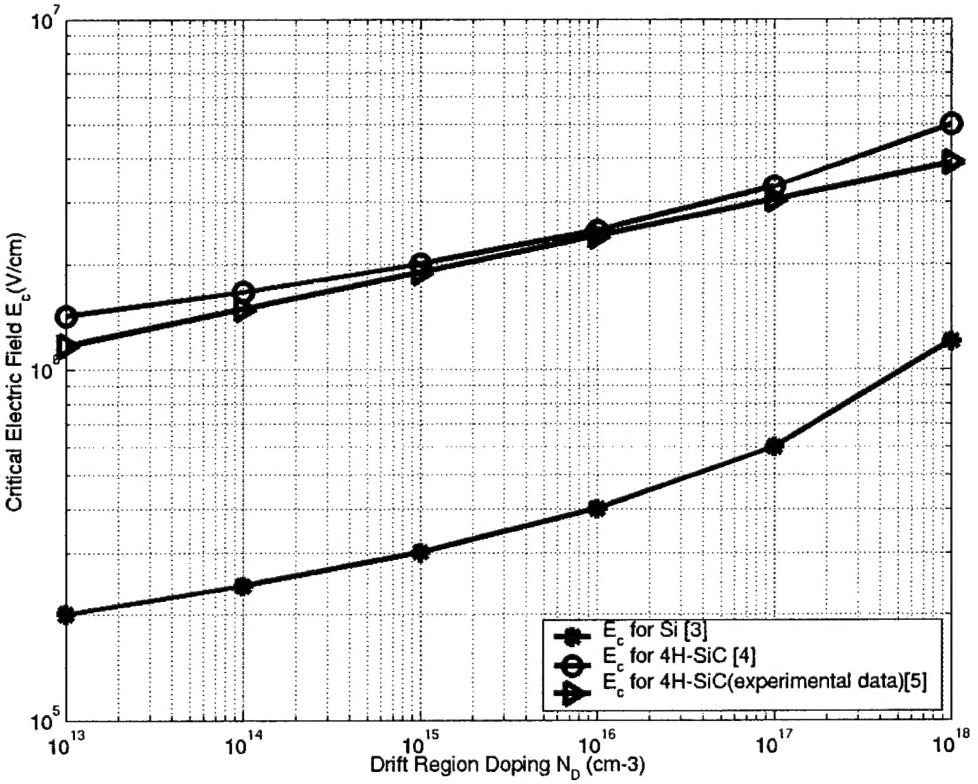


Fig. 1.1. Variation of critical electric field as a function of drift region doping for Si and 4H-SiC material [3], [4] & [5].

$R_{on,sp}$ varies as the square of the V_{BR} voltage and inversely proportional to the cube of E_c. Figure 1.2 shows a plot of $R_{on,sp}$ vs. V_{BR} for Si and 4H-SiC, and just switching from Si to 4H-SiC material, $R_{on,sp}$ gets 200 times smaller than comparable Si devices. Another useful performance measure for power MOSFETs is $V_{BR}^2 / R_{on,sp}$ (MW/cm^2), also known as the Figure of Merit (FOM), and we find that with SiC it is 200 times higher than similar Si power MOSFETs. $V_{BR}^2 / R_{on,sp}$ only depends on bulk mobility (μ_{bulk}), semiconductor dielectric constant (ε_{SiC}), and critical electric field (E_c). Thus, SiC power devices show higher breakdown voltages and lower power loss than Si devices.

1.1.3 High thermal conductivity

Table 1.1b

Property	4H-SiC	6H-SiC	Si	Cu
Thermal conductivity (W/cm^0K)	3.3	3.3	1.5	3.97

SiC is an excellent thermal conductor and has a high thermal conductivity close to Cu. Thus for high power/ high voltage SiC devices, device cooling and packaging is less expensive compared to Si devices. SiC substrates (good conductor) can be used in fabricating GaN LED's instead of sapphire (insulator), which may result in increased device performance.

1.1.4 High saturated drift velocity

Table 1.1c

Property	4H-SiC	6H-SiC	Si
Saturated drift velocity (cm/sec) V_{sat} @ $E=2\cdot10^5$ V/cm	$2\cdot10^7$	$2\cdot10^7$	$1\cdot10^7$

SiC material has two times higher saturated drift velocity for electrons flowing in the directions perpendicular to the c-axis [6] compared to Si at high fields. Thus SiC material is used in high power microwave devices operating in the GHz range.

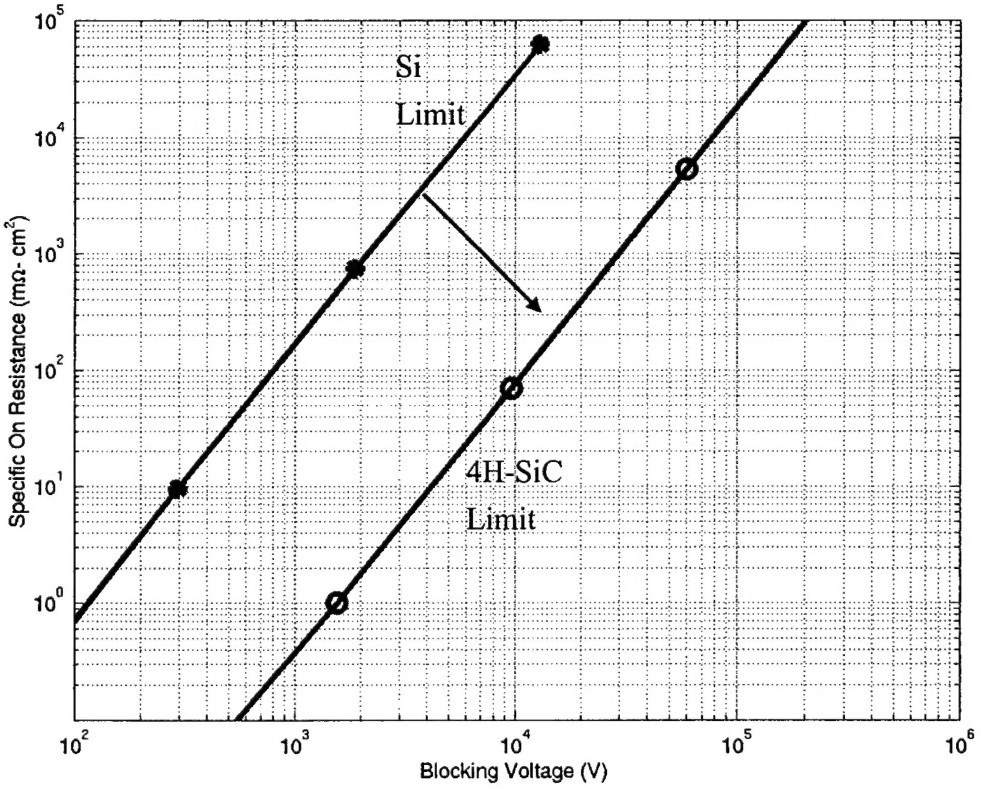


Fig. 1.2. Specific on-resistance and blocking voltage of silicon and 4H-SiC power MOSFET structures with a "non-punch-through" design.

1.1.5 Thermal oxide

SiC is the only compound semiconductor which can be thermally oxidized to grow high quality SiO_2 much like the Si/SiO_2 interface. This allows it to compete with standard Si-based MOS devices such as MOSFETs, IGBTs and MOS controlled thyristors.

1.1.6 Other properties [7],[8]:

Table 1.1d

Property	4H-SiC	6H-SiC	Si
Dielectric constant ε_{sic}	9.7	9.7	11.8
Mobility(cm^2/Vsec) $\mu_{n\ bulk}\ \perp$	800	400	1400
$\mu_{n\ bulk}\ \|\|$	900	100	1400

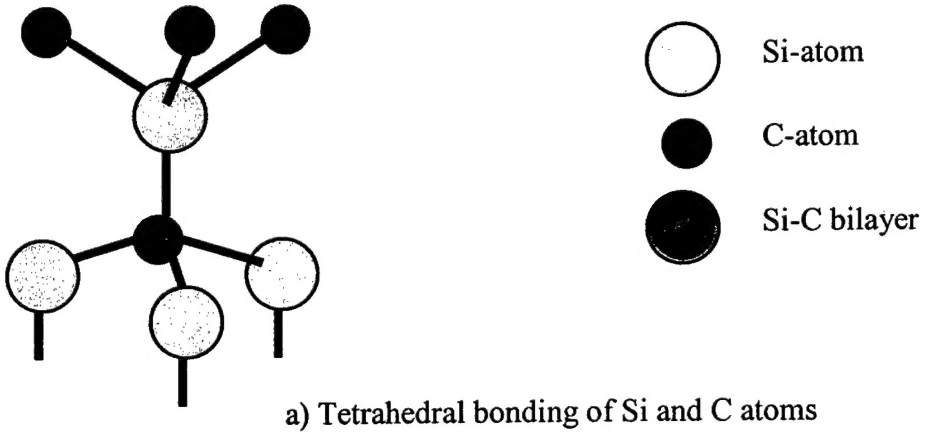
Because of its hardness, SiC is still used as a coating material for drill bits and saw blades. However, SiC has a lower bulk mobility, lower inversion layer mobility, and large defect-free single crystal wafers are still unavailable. Selective doping in SiC is achieved by ion implantation, and activation of dopants requires a high temperature processing step. The strong Si-C bond requires that all processing steps go on at a very high temperature. Also growing and maintaining a high quality SiC/SiO_2 interface is crucial for MOS device technology. Once these processing issues are solved, SiC material holds great promise as a power semiconductor material.

1.2 SiC Polytypes

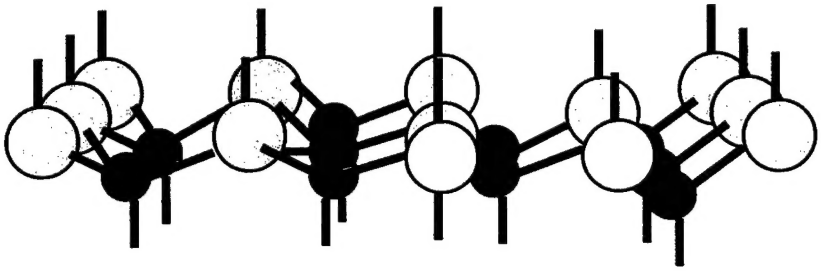
SiC is a wide bandgap semiconductor which exists in different polytypes. All polytypes consist of alternating hexagonal frames of Si and C atoms, with the C atom triply bonded and situated above the center of three Si atoms and also bonded with a Si atom belonging to the next layer. Every atom is tetrahedrally surrounded by four of the other species as shown in Fig. 1.3a. The most popular polytypes are 3C, 4H and 6H. Among them 3C is the only cubic polytype, also known as _-SiC, and 4H and 6H are hexagonal polytypes, also known as _-SiC. Figure 1.3b shows a hexagonal bilayer with Si and C in alternating tetrahedrally coordinated sites. As in Fig. 1.3c, if the first hexagonal double layer of Si and C atoms is labeled position A, then the next Si and C layer that lies offset from the first layer can only have either B or C position. The difference between polytypes is the stacking sequence along the c-axis of the successive Si-C double layers. Thus, different polytypes are formed by permutation of these three A, B, and C positions. For example, a repetitive stacking sequence of ABCABC.... forms the 3C-SiC (a 100% cubic or zincblende structure), ABAB... forms the 2H-SiC (a 100% wurtzite or hexagonal structure), ABCBABCB.... forms the 4H-SiC (a 50% cubic and 50% wurtzite structure) and lastly ABCACB .....forms 6H-polytype (a 33% wurtzite and 66% zincblende structure). Depending on the stacking sequence, the bonding between Si-C atoms in adjacent bilayers is either cubic (zincblende) or hexagonal (wurtzite) in nature. The stacking sequence for a particular polytype can be seen by looking at the cross-section of the crystal structure from the side $(11\bar{2}0)$. From the top all polytypes look the same, as they are stacked along the c-axis. Figure 1.4a), b), and c) show the stacking sequence for 3C, 4H and 6H-SiC polytypes, viewed in the $(11\bar{2}0)$ plane. Figure 1.4d) shows a model of the 4H-SiC crystal structure showing the stacking sequence [9].

1.3 Report Outline

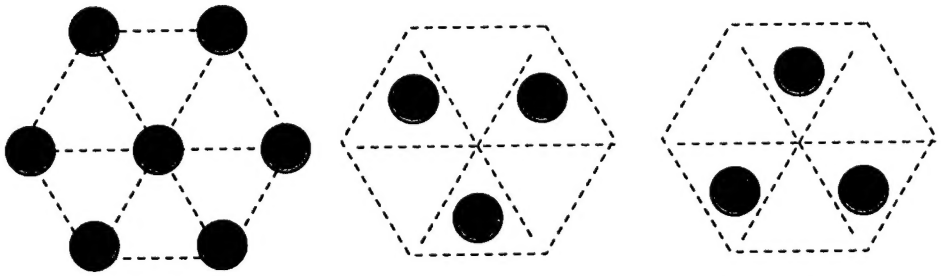
The goal of this project was to reduce the channel resistance of a 4H-SiC power DMOS structure. Chapter 2 addresses some of the technological problems associated with the 4H-SiC DMOS structure. In this thesis, three different types of DMOS designs were investigated. Initially we wanted to avoid p-type implants and high-temperature implant activations, and two new structures, namely, the "etched epitaxial base DMOS"



a) Tetrahedral bonding of Si and C atoms

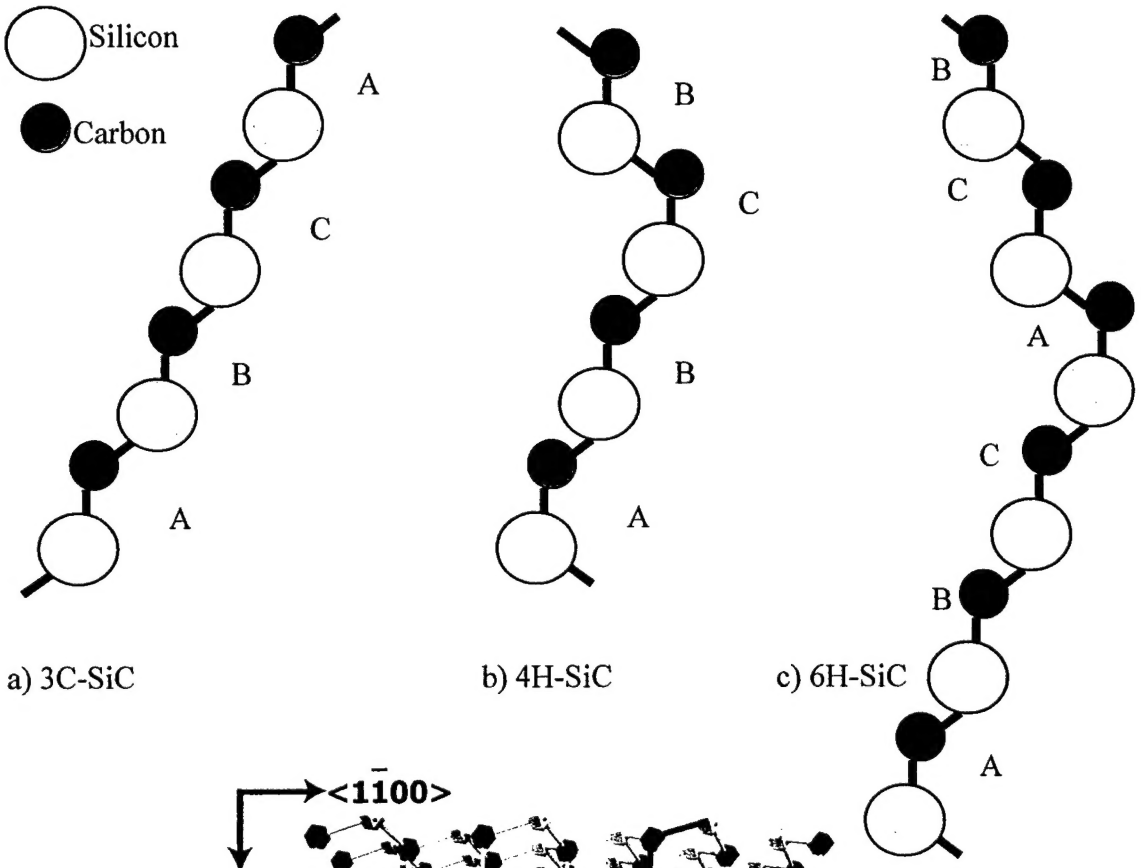


b) A hexagonal bilayer of Si and C atoms

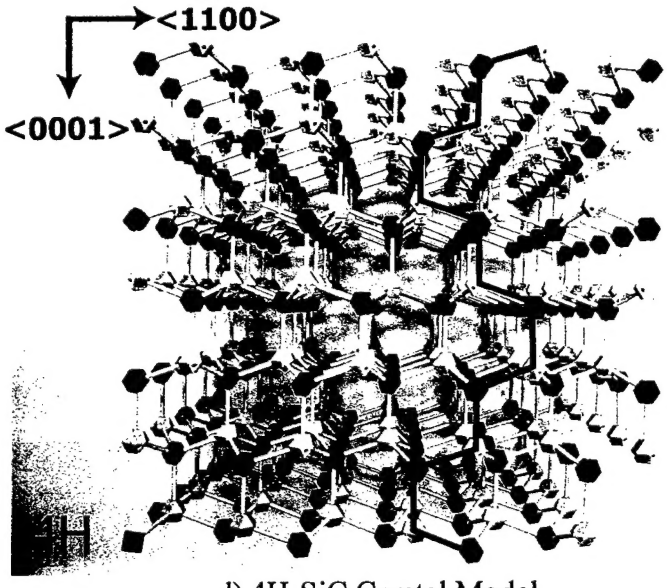


c) A plane of atoms

Fig. 1.3. Atomic structure of SiC: a) tetrahehral bonding of Si and C atoms; b) hexagonal bilayer of Si and C atoms tetrahedrally bonded; c) Si-C bilayers in A, B, and C positions.



a) 3C-SiC b) 4H-SiC c) 6H-SiC



d) 4H-SiC Crystal Model

Fig. 1.4. The stacking sequence in the $(11\bar{2}0)$ plane of a) 3C-, b) 4H-, and c) 6H-SiC polytypes; d) a 4H-SiC crystal model in the $(11\bar{2}0)$ plane [9].

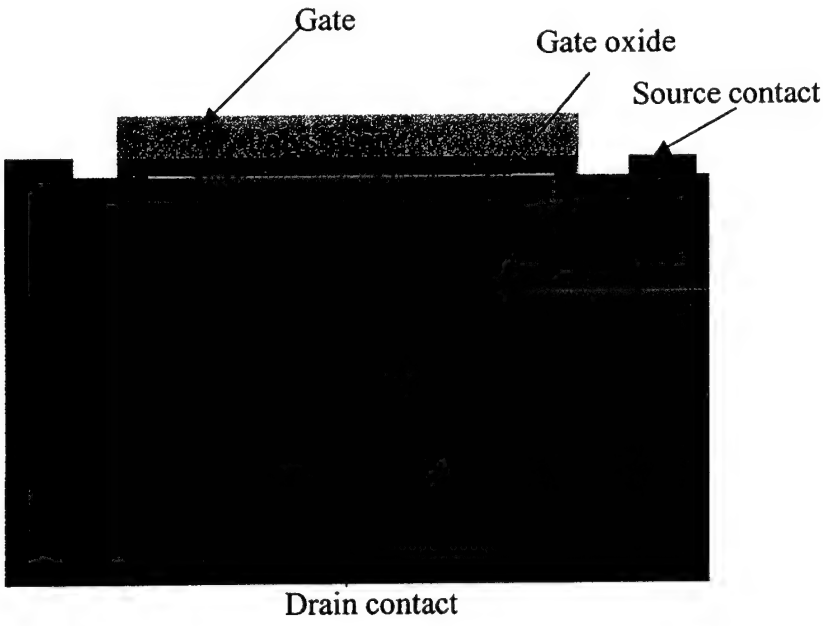
and the "implanted epitaxial base DMOS" were introduced. Chapter 3 presents the simulation, design, and fabrication of the "etched epitaxial base DMOS" structure. Chapter 4 deals with the "implanted epitaxial base structure". Ongoing researches on 4H-SiC MOS structures show significant improvements to the inversion channel mobility when activating the implants in a silane ambient. To reduce the channel resistance further, the "short-channel counter-doped self-aligned DMOS" structure was introduced. Chapter 5 deals with the simulations on this structure and Chapter 6 describes the process developments for the fabrication of the short channel counter-doped self-aligned 4H-SiC DMOS structures. Chapter 7 presents the fabrication details and Chapter 8 discusses the experimental results obtained. The conclusions of this research are given in Chapter 9 along with some recommendations for future work.

2. SIC POWER MOSFETS

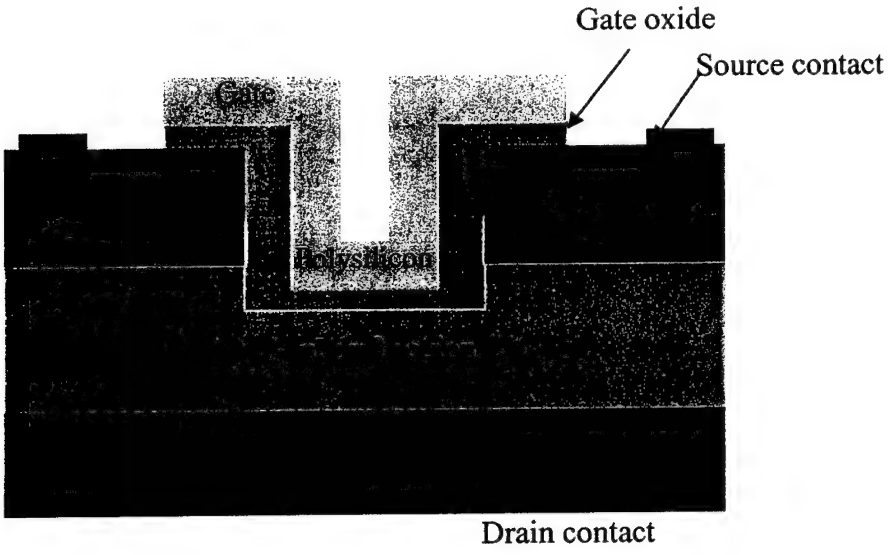
2.1 Motivation for SiC Power MOSFETs

SiC power MOSFETs are attractive because of their low on-resistance, high blocking voltage capability, and high switching speed compared to Si-based power devices. Power MOSFETs are inherently capable of operating at very high frequencies compared to bipolar power switches like the BJT, due to absence of minority carrier transport. Also, high input impedance greatly simplifies the gate drive circuitry. The ability to function under extreme high temperature, high power, and high radiation environments makes SiC based electronics suitable in a variety of applications like power supplies, traction vehicles, industrial motors, electric vehicles, military systems, aerospace applications, and in nuclear power reactors.

Power MOSFETs are switches which have the ability to produce large on-currents during the on-state and can support large breakdown voltages during the off-state. Vertical power MOSFETs in SiC come in two types: DMOS (double implantation) and UMOS (U-shaped) structures. Both MOSFETs have a lightly doped n^- layer to form the drift region, epitaxially grown on an n^+ substrate which acts as the drain contact. In the UMOSFET, a p-type base epilayer is then grown on top of the drift region, whereas in DMOS the p-type base is formed by ion implantation of boron or aluminum. The n^+ sources are then formed by ion implantation of nitrogen or phosphorus. In the DMOS structure, the channel then forms on the (0001) surface. On the other hand, in the UMOS structure, a U-shaped trench is formed by reactive ion etching (RIE) of SiC, and the channel forms on the side-wall of the trench. Figure 2.1 shows the cross sections of SiC DMOS and UMOS power transistors. One advantage of the UMOS structure over the DMOS structure is that it does not have any JFET region, which is inherent in the DMOS structure, and therefore can have a lower specific on-resistance with higher channel density compared to the DMOS structure. However, in UMOS, the RIE technique used to form the U-shaped trench results in a roughened side wall and can reduce the channel mobility by surface roughness scattering [10]. Also high electric



a) DMOS structure



b) UMOS structure

Fig. 2.1. Cross-sections of DMOS and UMOS power transistors in SiC.

fields can arise at the trench corners that can lead to premature oxide breakdown. The oxide can be protected by implanting a bottom p^+ region, but this introduces a JFET region between the p-base and p^+ bottom implant [11].

2.2 Conventional DMOSFET

Figure 2.1a shows the n-channel DMOS structure consisting of n^- drift region on an n^+ substrate. The distance between two p-wells is the length L_{JFET}, and the channel length L_{ch} is the distance between the edge of the n^+ source and the p-well. In the on-state, a positive voltage applied to the gate forms a channel between the n^+ source and n^- drift region, and with a positive voltage on the drain, current flows through the channel and drift region. The current flow is determined by the $R_{on,sp}$ (R.A) consisting of the channel resistance ($R_{ch,sp}$), the JFET resistance between the two p-wells ($R_{JFET,sp}$), and the n^- drift region resistance ($R_{drift,sp}$), neglecting the contact and substrate resistances.

$$R_{on,sp} = R_{ch,sp} + R_{JFET,sp} + R_{drift,sp} \tag{2.1}$$

If the L_{JFET} length is large, then the JFET region resistance can also be neglected and the $R_{on,sp}$ is given as,

$$R_{on,sp} = R_{ch,sp} + R_{drif,spt} \tag{2.2}$$

$$R_{ch,sp} = \frac{L_{ch}S}{C_{ox}\mu_{ch}(V_G - V_T)} \tag{2.3}$$

$$R_{drift,sp} = \frac{W_D}{q\mu_{bulk}N_D} \tag{2.4}$$

where L_{ch} is the channel length , S is the cell pitch, C_{ox} is the oxide capacitance, μ_{ch} is the inversion channel mobility, V_G is the gate voltage, V_T is the threshold voltage, W_D is the drift region thickness, q is the charge, μ_{bulk} is the mobility in the drift region, and N_D

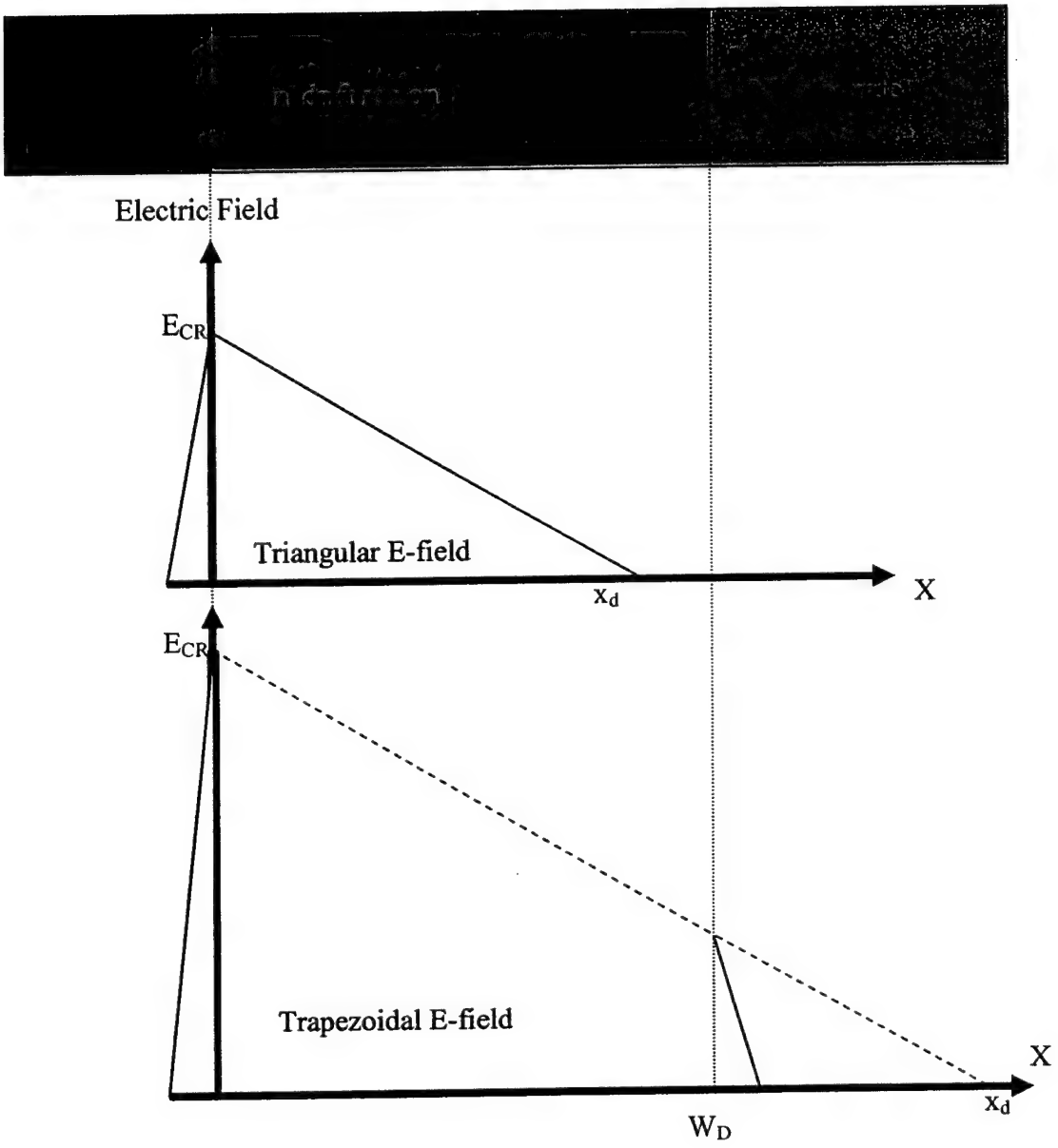


Fig. 2.2. Electric fields in the DMOS structure.

is the drift region doping. In the blocking mode of operation or off-state, the p-base, n^+ source, and gate all are grounded. The blocking voltage is supported mainly across the n^- drift region, and therefore this drift region is very lightly doped. The p-base has a retrograde doping profile. This means that near the SiC/SiO_2 interface it is lightly doped ($\sim 5 \cdot 10^{16}$ cm^{-3}) in order to maintain an easy turn on ($V_T \sim 2$-$3V$), and the doping concentration deep into the well is kept sufficiently high ($\sim 1 \cdot 10^{18}$ with 1% activation) to prevent punch through from the n-type drift region to the source. The blocking voltage for a i) triangular electric profile (when the drift region is not fully depleted) and ii) a trapezoidal electric profile (when the drift region is fully depleted) are shown in Fig. 2.2, and the necessary equations are given as,

i) Triangular electric field: $x_d < W_D$

$$V_{BR} = \frac{1}{2} E_c x_d = \frac{\varepsilon_{SiC} E_c^2}{2qN_D} \tag{2.5}$$

ii) Trapezoidal electric field: $x_d > W_D$

$$V_{BR} = \left(E_c - \frac{qN_D W_D}{2\varepsilon_{SiC}} \right) W_D \tag{2.6}$$

Figure 2.3 shows a design chart for vertical DMOS/UMOS power MOSFETs using the relationship between $R_{on,sp}$ and V_{BR} as a function of the drift region thickness (W_D) and doping (N_D), with W_D varying from 10 to 150 μm and N_D varying from $1 \cdot 10^{14}$ to $1 \cdot 10^{17}$ cm^{-3}. From the chart we find that for a 10 μm drift region thickness and a doping of $1 \cdot 10^{15}$ cm^{-3}, the V_{BR}= 1800V and $R_{on,sp}$= 7 mΩ-cm^2. With the same doping and for a 50 μm epilayer the blocking voltage is increased to 7100V with $R_{on,sp}$= 34 mΩ-cm^2, and for 100 μm, V_{BR}= 9600V and $R_{on,sp}$= 68 mΩ-cm^2. At this doping level no more voltage gain is possible going to a 150 μm epilayer curve, as shown in the figure.

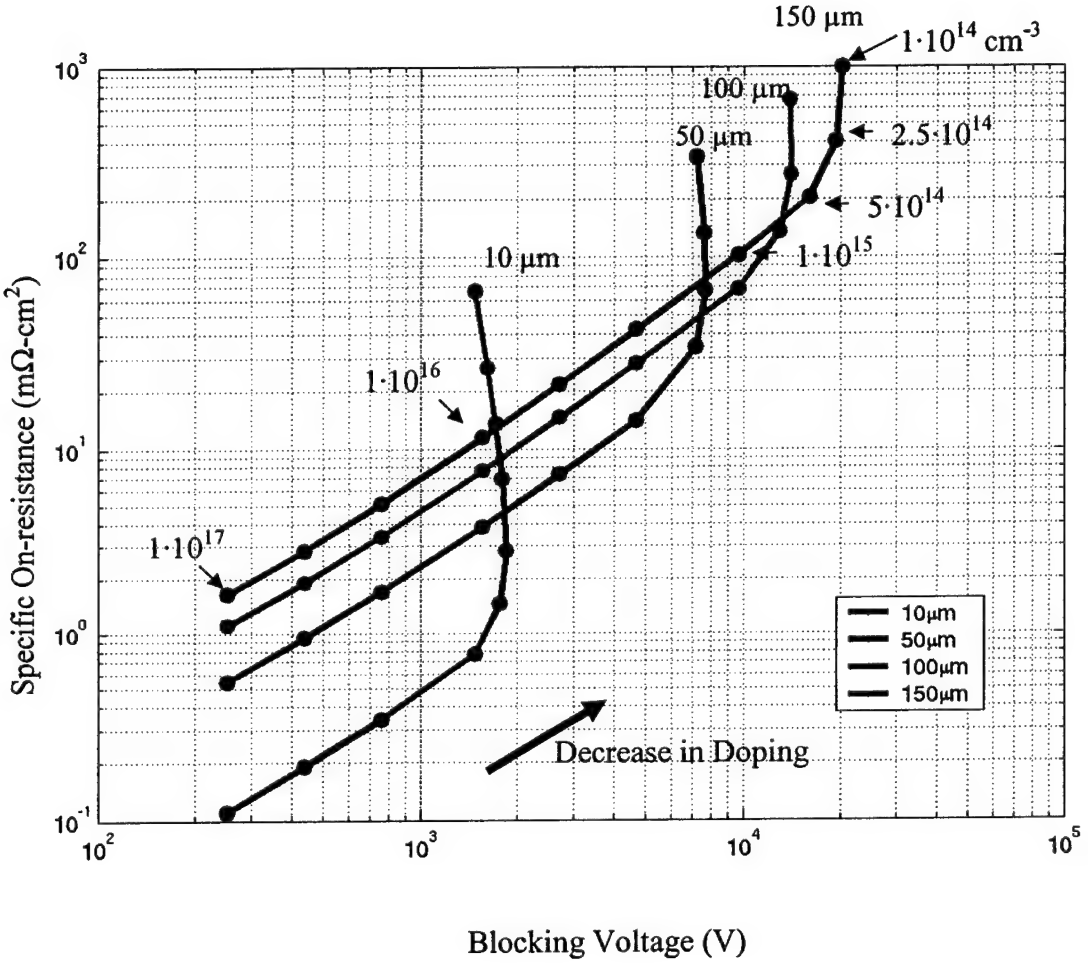


Fig. 2.3. Vertical power DMOS design chart showing specific on-resistance versus blocking voltage. Here, each curve corresponds to a different epilayer thickness, and each point on each curve corresponds to a different doping.

2.3 Technological Problems of 4H-SiC DMOSFETs

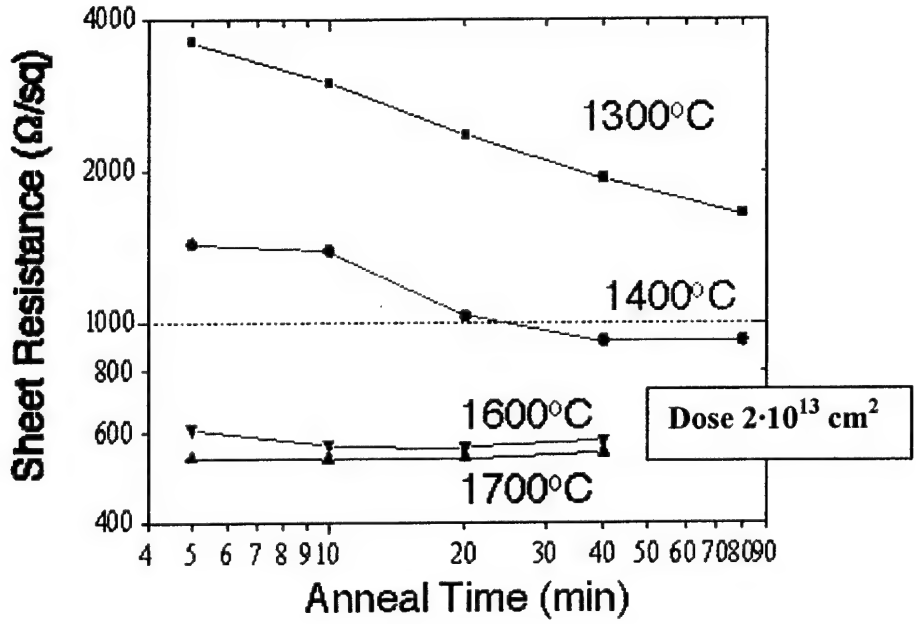
4H-SiC is extremely attractive for power MOSFET applications because of its wide bandgap, high critical electric field, and high thermal conductivity. 4H-SiC power MOSFETs offer higher blocking voltage, higher switching speed, lower loss, smaller device size and higher operating temperature range compared to Si power MOSFETs. However, all these advantages have yet to be realized in experimental SiC devices. In order to obtain commercial success for SiC power MOSFETs, some technological difficulties need to be solved before 4H-SiC material can achieve its true potential. The processing issues related to the fabrication of 4H-SiC power DMOSFETs include: 1) high implant activation temperatures which lead to surface degradation, 2) low inversion channel mobilities and consequently high specific on-resistances, and 3) high leakage currents and low breakdown voltages of large area power devices due to crystal defects.

2.3.1 High implant activation temperatures

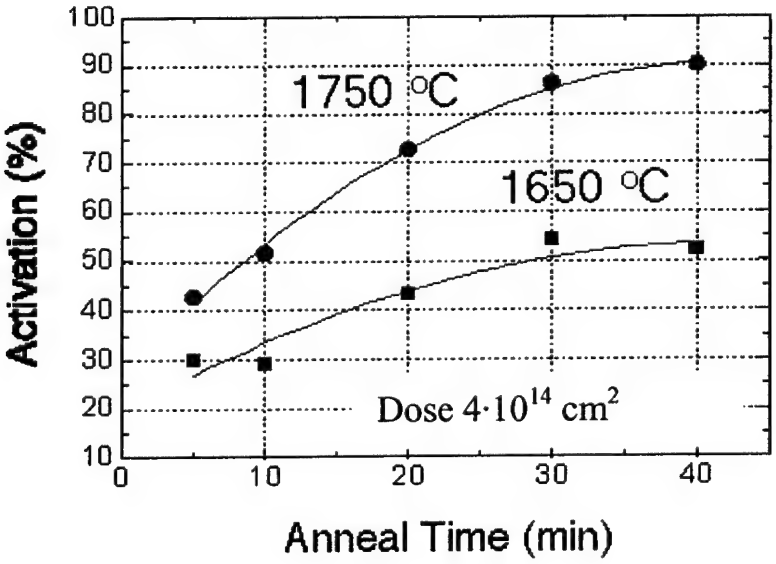
In SiC, selective doping is performed by ion implantation. The activation of the dopants is achieved by a high temperature anneal in an inert ambient. For the source implants, nitrogen is implanted at an elevated temperature of approximately 650°C and then subsequently annealed at a high temperature to remove lattice damage and activate the dopants. Figure 2.4a shows a plot of the sheet resistance (Ω/□) of nitrogen implanted into 4H-SiC vs. anneal time and temperature. The plot shows that to obtain a sheet resistance of 1000 Ω/□, the required anneal temperature is between 1400 to 1700 °C [12]. The p-base is then formed by implantation of boron into SiC. Figure 2.4b shows a plot of the activation percentage of boron into 4H-SiC vs. anneal time and temperature. The plot reveals that to obtain 90% activation, the anneal temperature must be greater than 1750°C [13].

2.3.2 Low inversion channel mobility

The 4H-SiC polytype is the polytype of choice for power MOSFET applications as it has higher bulk mobility and less mobility anisotropy than the 6H-polytype. However, the inversion channel mobility measured from lateral or planer 4H-



a) Sheet resistivity of nitrogen into 4H-SiC

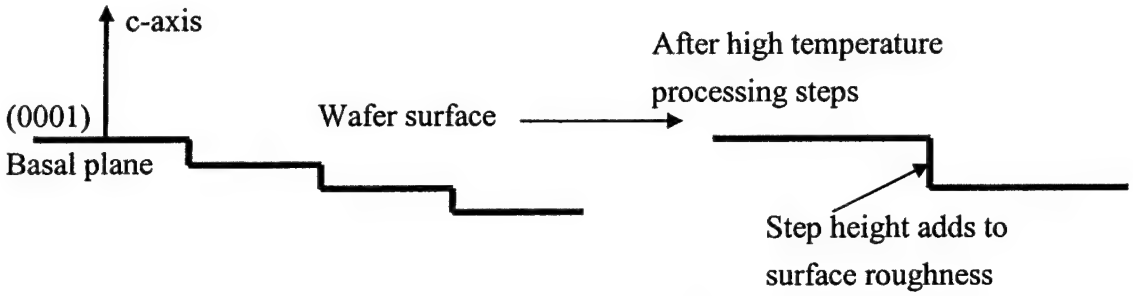


b) Activation percentage of boron into 4H-SiC

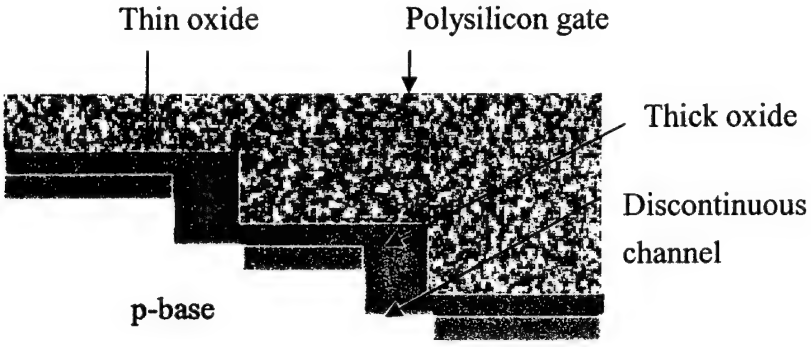
Fig. 2.4. Sheet resistivity of nitrogen implantation and activation percentage of boron implantation into 4H-SiC as a function of time and anneal temperature [12], [13].

SiC MOSFET test structures is only 2-9 cm^2/Vsec, while it is in the range of 80-100 cm^2/Vsec on 6H-SiC MOSFETs [10], [14]. This low value of inversion layer mobility is obtained from lateral MOSFETs with the channel forming on a p-epilayer and requiring a source implantation only (overall anneal temperature ~1400°C). A channel mobility less than 1 cm^2/Vsec is not at all uncommon on 4H-SiC MOSFETs when the channel is formed on implanted p-base regions (overall anneal temperature ~1700°C). Since the 4H-DMOS structure requires a p-base implantation, the channel formed on the implanted region has a degraded channel mobility.

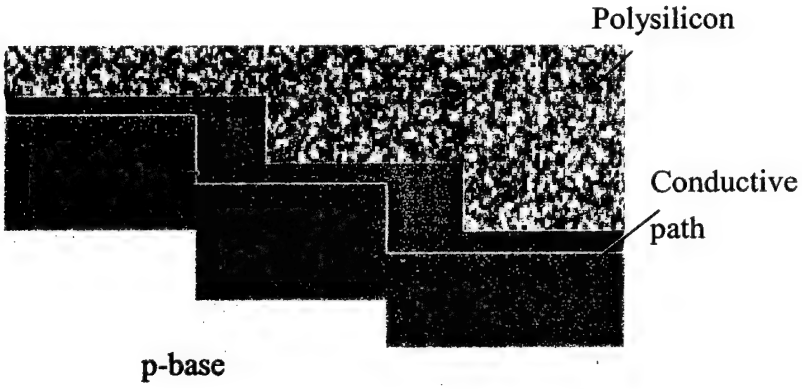
Capano et al. [15] has shown that p –type implantation into 4H-SiC followed by a high temperature implant activation step can cause a surface roughness phenomenon called "step bunching" due to loss of silicon from the surface. This surface degradation can lead to extremely low inversion channel mobility in 4H-SiC DMOS transistors. SiC wafers are routinely cut at an angle of 3.5° (6H) and 8° (4H) from the basal plane, and these steps (~$10A^0$) provide the necessary information for the step flow growth in which the respective epitaxial layers are grown [16]. At high annealing temperatures (1700^0C for p-type base implant), sublimation of Si can occur, and the surface goes to a lower energy state as the density of the steps is decreased while the step height (~250°A) is increased by creating larger steps. Due to the oxidation anisotropy of the SiC lattice [17], where the carbon face (a-face) oxidizes at faster rate than the silicon face (c-face), a series of thick and thin oxides in the stepped surface can thus form, as shown in Fig. 2.5a and b. When MOSFETs are formed on these surfaces, the difference in gate oxide thickness can form discontinuous channels which act as potential barriers to current flow during the on-state. From a literature study, we find that the best mobility values for 4H-SiC MOSFETs can be obtained when the implant activation temperature is kept low, in the range 1200 to 1300°C [18],[19]. Unfortunately, the high dose p-type boron implantation required for power DMOSFETs is not activated properly (activation < 1%). Moreover, Afanasev et al. [20] has also shown that 4H-SiC material has a high interface state density near the conduction band edge compared to the 6H-polytype. Thus the low inversion channel mobility results in high $R_{on,sp}$ in power DMOSFETs, and Fig. 2.6 shows a plot of $R_{on,sp}$ vs. V_{BR} for channel mobilities of 5 to 50 cm^2/Vsec.



a) Step bunching in SiC



b) Inversion channel FET showing discontinuous channel



c) ACCUFET showing a continuous channel

Fig. 2.5. a) Step bunching in SiC, b) inversion channel FET, and c) ACCUFET.

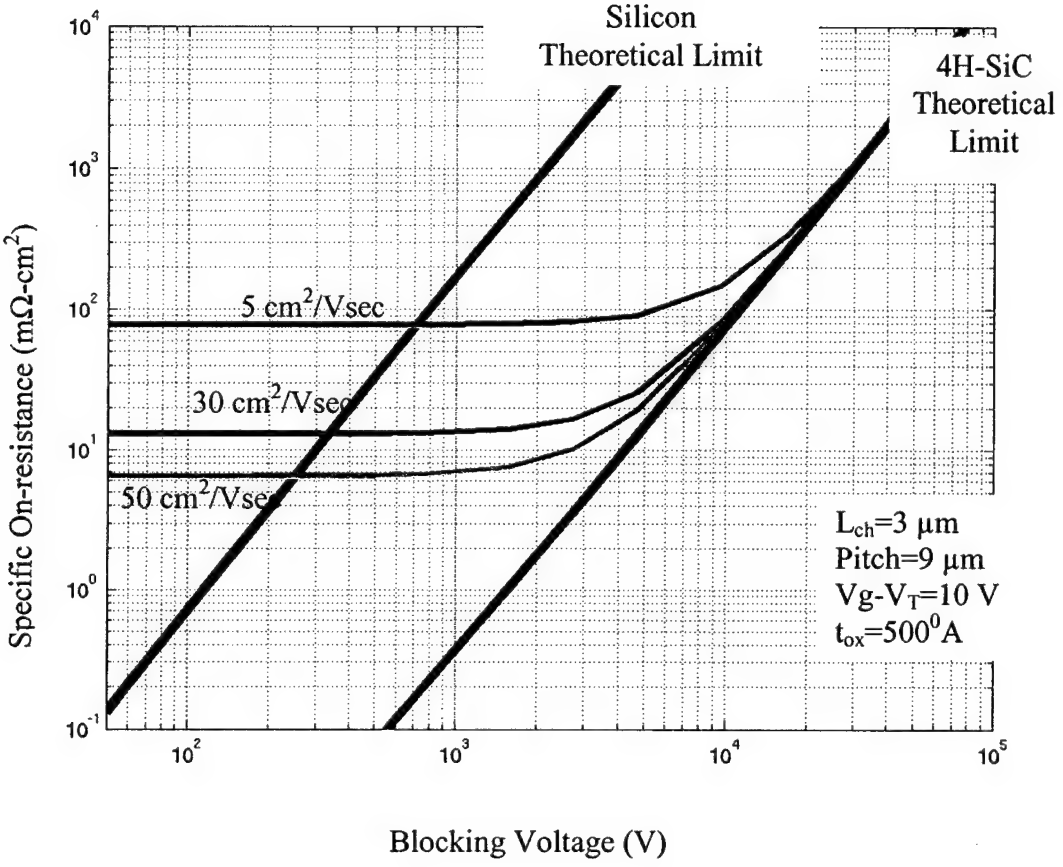


Fig. 2.6. Effect of inversion channel mobility on the specific on-resistance. With a μ_{ch} of 5 cm^2/Vsec the 4H-SiC high voltage devices (<10 kV) will be limited by the resistance from the channel region.

One possible solution to this problem is to convert the inversion channel FET to an accumulation channel FET by providing an n-type conductive path. The main features of ACCUFETs include an n- type channel region. The thickness and doping of the n type layer is carefully chosen such that the channel region is completely depleted from the depletion regions of the p-type base and the polysilicon gate, and the device is thus normally off. The accumulation channel FETs exhibit a higher mobility value than the inversion FETs, as they provide a continuous conductive path around the potential barriers associated with the steps as shown in Fig. 2.5. Shenoy et al. [21] has reported a 6H DMOS ACCUFET with on-resistance as low as 18 $m\Omega\text{-}cm^2$ and inversion channel mobility as high as 81 $cm^2/V\text{-}sec$. The overall implant activation temperature was kept at 1400°C. Tan et al. [11] has demonstrated a 1400 V UMOS ACCUFET in 4H-SiC with a specific on-resistance of 15.7 $m\Omega\text{-}cm^2$, where the implants were annealed at 1600°C. One disadvantage of an ACCUFET as a power device is that the threshold voltage is difficult to control and is close to zero (V_T~0 to 1 V), and may become normally on (V_T ~negative) at high temperatures. Thus, they may not be suitable for high power/high temperature electronics.

2.3.3 Low breakdown voltages

High blocking voltage can be achieved by fabrication of devices on thick epilayers with appropriate dopings. With a high wafer quality, better surface morphology with fewer micropipes, fewer pits and asperities, the device yield can be increased significantly. Micropipes penetrating a high voltage pn junction can destroy the junction's ability to block voltage. Improvements in SiC substrate quality are therefore necessary in order to have SiC power MOSFETs commercially available.

2.4 Evolution of SiC power MOSFET's

Figure 2.7 shows a performance plot of the best reported inversion and accumulation channel power MOSFETs to date in terms of V_{BR} and $R_{on,sp}$. In 1996, the first vertical 6H-SiC DMOSFET on a 10 μm drift layer was reported by Jayarama N. Shenoy [22] of Purdue University with V_{BR} of 760V, $R_{on,sp}$ of 125 mΩ-cm^2, and a V_{BR}^2 / $R_{on,sp}$ of 4.6 MW/cm^2. In 1997, Cassady et al [10] of Northrup Grumman with a 25 μm thick epilayer demonstrated V_{BR} of 1400V, $R_{on,sp}$ of 433 mΩ-cm^2, and V_{BR}^2 / $R_{on,sp}$ of 4.5 MW/cm^2 on their 4H-UMOS devices. Shenoy et al [21] in 1997 introduced a 6H accumulation channel DMOSFET with a V_{BR} of 350V, $R_{on,sp}$ of 18 mΩ-cm^2, and V_{BR}^2 / $R_{on,sp}$ of 6.8 MW/cm^2. In 1998, Jian Tan of Purdue University [11] reported a 1400V 4H-UMOS ACCUFET device with a $R_{on,sp}$ of 15.7 mΩ-cm^2 and V_{BR}^2 / $R_{on,sp}$ of 125 MW/cm^2. In 2000, Peters et al [23] of Seimens demonstrated 1800V, 47 mΩ-cm^2, and V_{BR}^2 / $R_{on,sp}$ of 70 MW/cm^2 on a 6H DMOSFET. In ISPSD' 2000, Kansai Electric Power Company together with Cree [24] reported a 4H-SiC SIAFET (Static Induction Injected AFET) with 4.5 kV and 387 mΩ-cm^2 on a 50 μm epilayer. Later in ICSCRM 2001, the same group reported a 5kV 4H-SiC SEMOSFET (Static Channel Expansion FET) with a specific on-resistance of 88 mΩ-cm^2 [25]. In ICSCRM 2001, Yu Li [26] of Purdue University demonstrated a 4H-SiC UMOSFET blocking 3kV with a specific on-resistance of 121 mΩ-cm^2 on a 50 μm drift region. Later in ISPSD 2002, Imran Khan of Purdue University [27] reported a 5kV, 105 mΩ-cm^2 UMOS device with a V_{BR}^2 / $R_{on,sp}$ of 243 MW/cm^2 on a 100 μm drift region. The 5kV UMOSFET maintained the low specific on-resistance value for current densities higher than 100 A/cm^2, unlike the SEMOSFET which saturated near 40 A/cm^2.

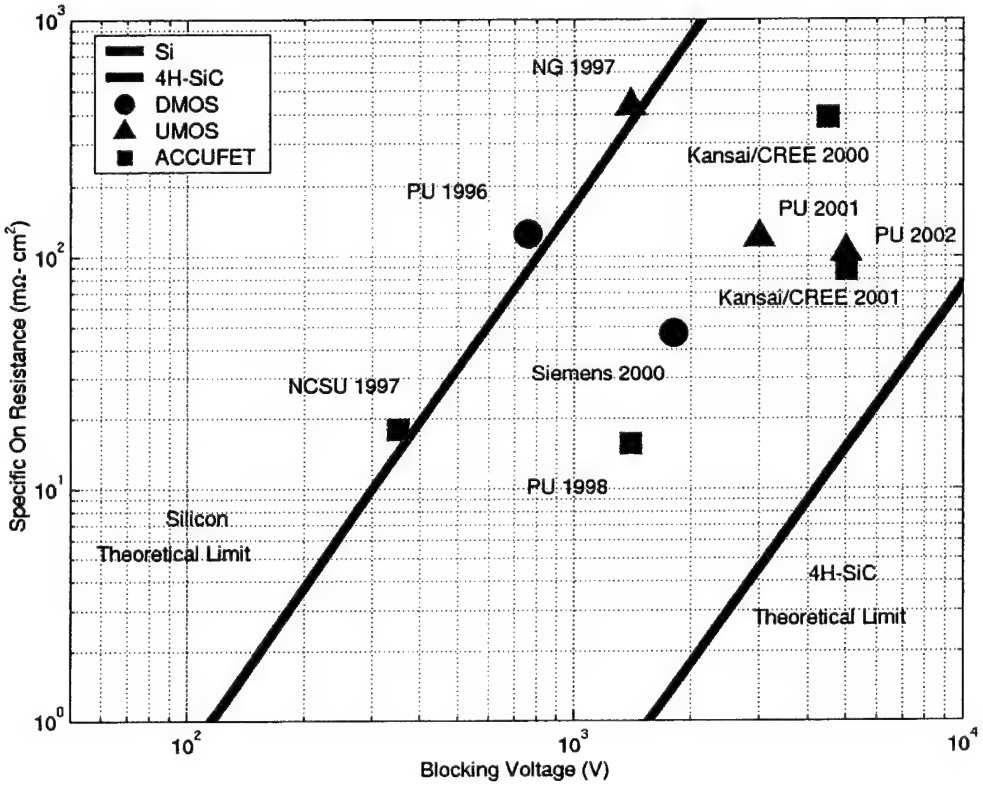


Fig. 2.7. Performance of SiC power MOSFETs.

3. EPITAXIAL BASE DMOSFET STRUCTURE: MOTIVATION, SIMULATION, FABRICATION, AND RESULTS

3.1 Motivation for an Epitaxial Base DMOSFET Structure

Conventional 4H-SiC DMOSFETs (D-doubly implanted) suffer from high specific on-resistances. This is because the activation of the p-type base implantation requires a high temperature (~1700^{0}C) annealing step which creates surface roughness, and inversion channel mobility gets extremely low. Figure 3.1 shows goals for future developments of 4H-SiC power DMOSFETs. To demonstrate a high voltage, high current and low loss power DMOSFET structure, we need to fabricate MOSFETs on thick drift regions with appropriate dopings, having low specific on-resistances, and with large active areas for high on-currents.

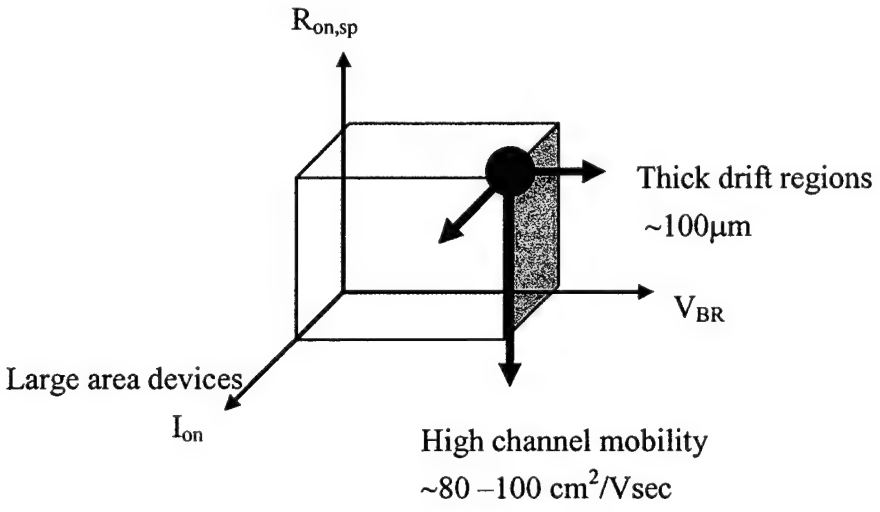


Fig 3.1. 4H-SiC power DMOSFET future goals.

To decrease the $R_{on,sp}$, the 4H-MOSFET channel mobility should be at least comparable to the 6H channel mobility (80-100 cm^2/Vsec). Implant activation temperature is an important parameter for MOSFET mobility because of its effect on surface roughness. A literature review on 4H mobility leads us to a solution of keeping the overall processing temperature below 1200°C, which is to avoid p type implants wherever possible. A new etched epitaxial base DMOS (epiDMOS) structure is introduced which uses two p-type epilayers to serve as the base and channel regions instead of a p-type retrograde implant.

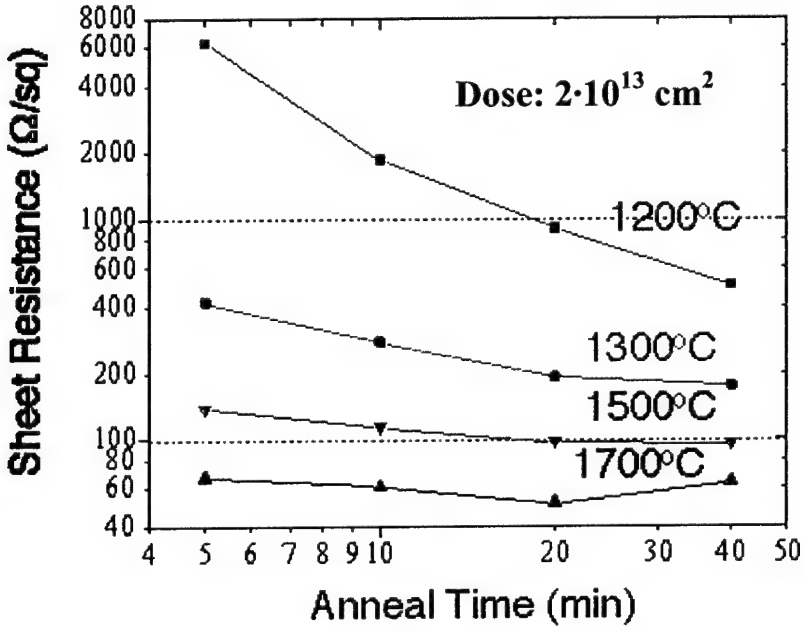


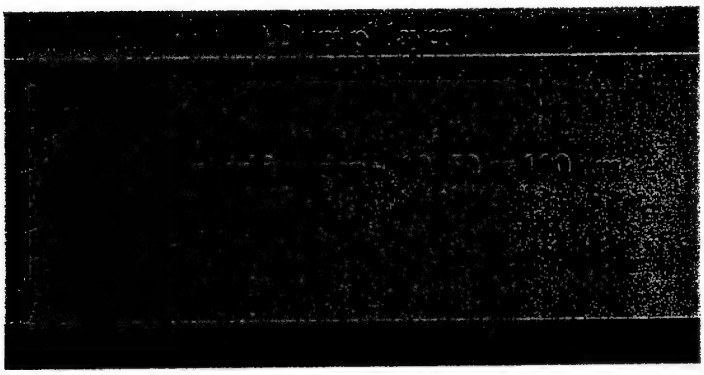
Fig. 3.2. Sheet resistivity of phosphorous implantation into 4H-SiC as a function of anneal time and temperature [12].

Figure 3.2 shows a plot of sheet resistance vs. anneal time and temperature for implantation of phosphorus into 4H-SiC. A sheet resistance less than 1000 Ω/□ can be obtained by annealing the phosphorus implant at 1200^0C [12]. Thus, the use of phosphorus as source implant instead of nitrogen will help us keep the overall process temperatures below 1200°C in order to alleviate the surface roughness phenomenon [15],[18],[19].

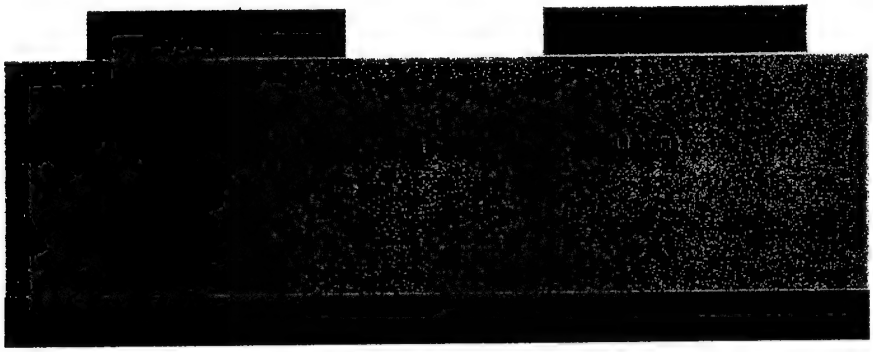
3.2 A 4H-SiC Etched Epitaxial Base (epiDMOS) DMOSFET structure

The process flow for fabrication of an etched epitaxial base DMOSFET is described in Fig. 3.3. The special features are stated below:

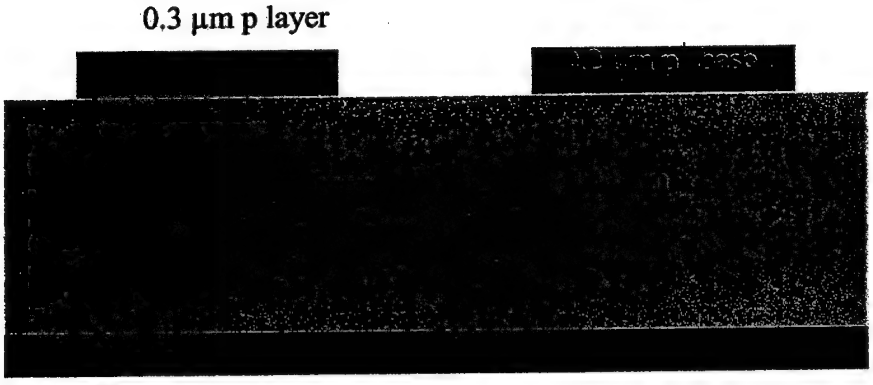
1) In this design the retrograde p-type implant step is replaced by two p-type epi growths. First a 0.2 μm, $5 \cdot 10^{18}$ cm^{-3} p^+ epilayer is grown on a 100 μm, $1 \cdot 10^{15}$ cm^{-3} n^- epi (see Fig. 3.3a) and is patterened and selectively etched by RIE (see Fig. 3.3b). This layer is for preventing punch through during high blocking state. It also serves as the contact region for the p-base. The second p epi is 0.3 μm thick and has a doping of $5 \cdot 10^{16}$ cm^{-3} for easy turn on (see Fig. 3.3c).
2) Phosphorus is used as the shallow n^+ source implant (see Fig. 3.3d) and activated at 1200^0C.
3) A nitrogen n^- plug implantation is then performed to a depth of 0.5 μm with doping profile sufficient to compensate the p epi doping and to have sufficient activation at a temperature of 1200°C. This region will connect the channel to the drain (see Fig. 3.3e).
4) 0.3 μm of the p-type channel region is etched to get to the p^+ base to form the p-type contacts (see Fig. 3.3f).
5) Each device is then separated by trench isolation (see Fig. 3.3g).
6) Heavily doped phosphorus source implants oxidize at a faster rate during the thermal gate oxidation step, and therefore a deposited poly oxide is used as gate and field oxide (see Fig. 3.3h).
7) The overall processing temperature is kept below 1200°C and the MOS channel forms on a p epilayer.



a) Starting wafer structure

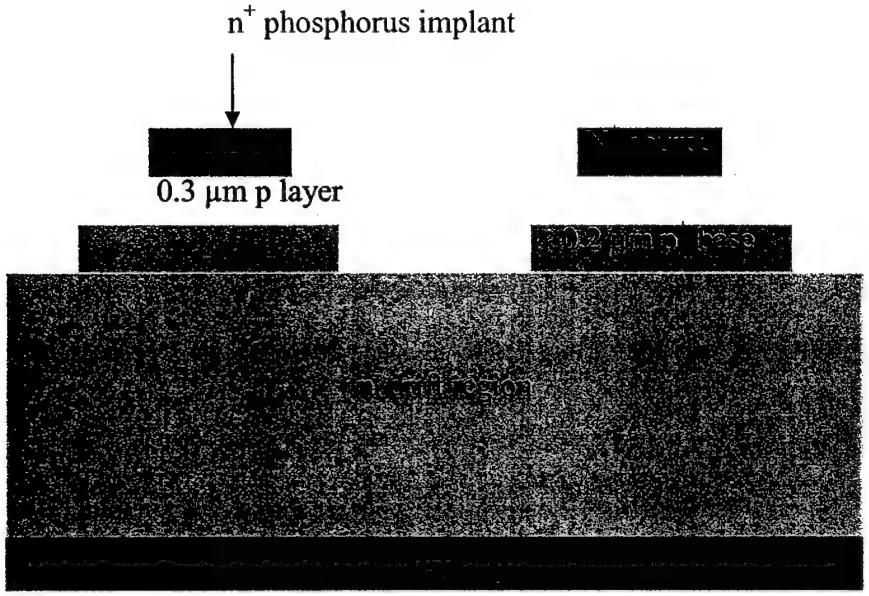


b) After patterning p^+ layer

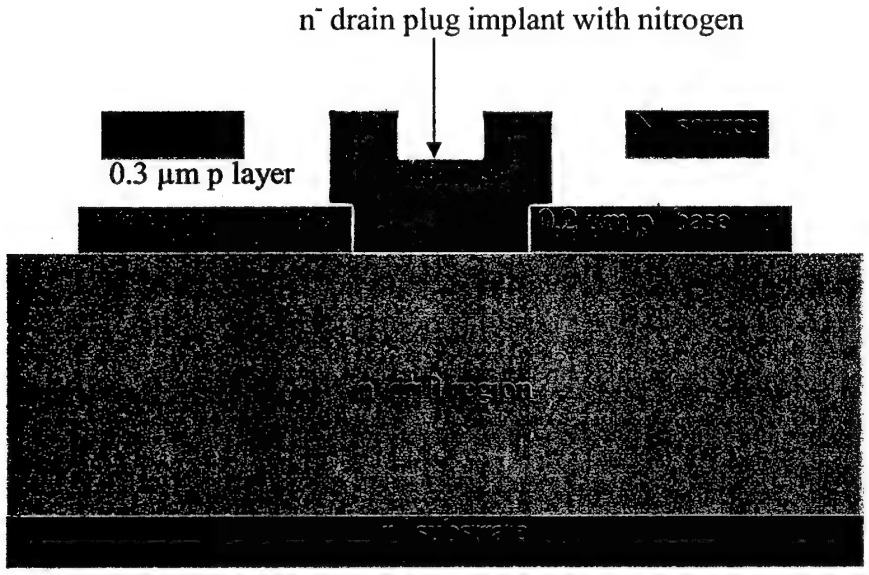


c) After epi growth of p layer

Fig. 3.3. Process flow of epiDMOS structures (continued).

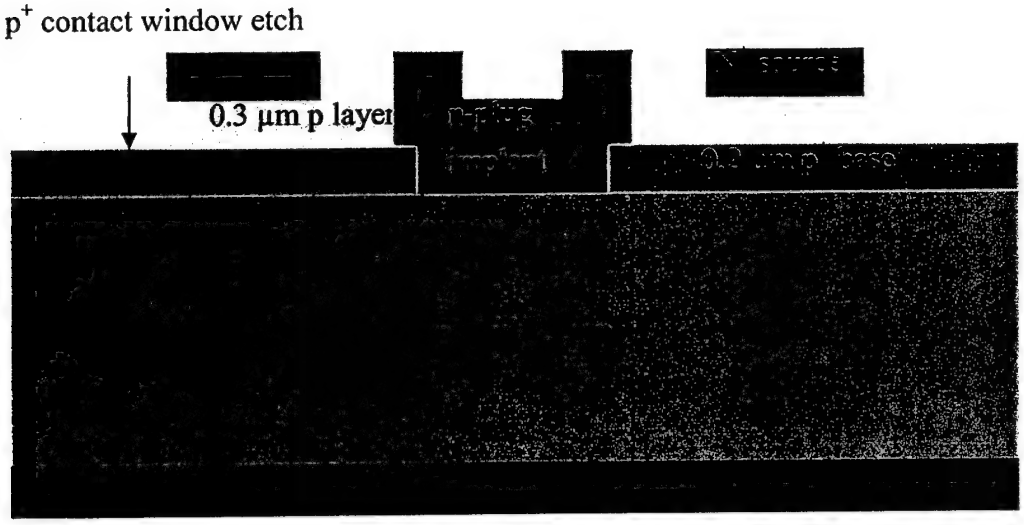


d) After n^+ source implants

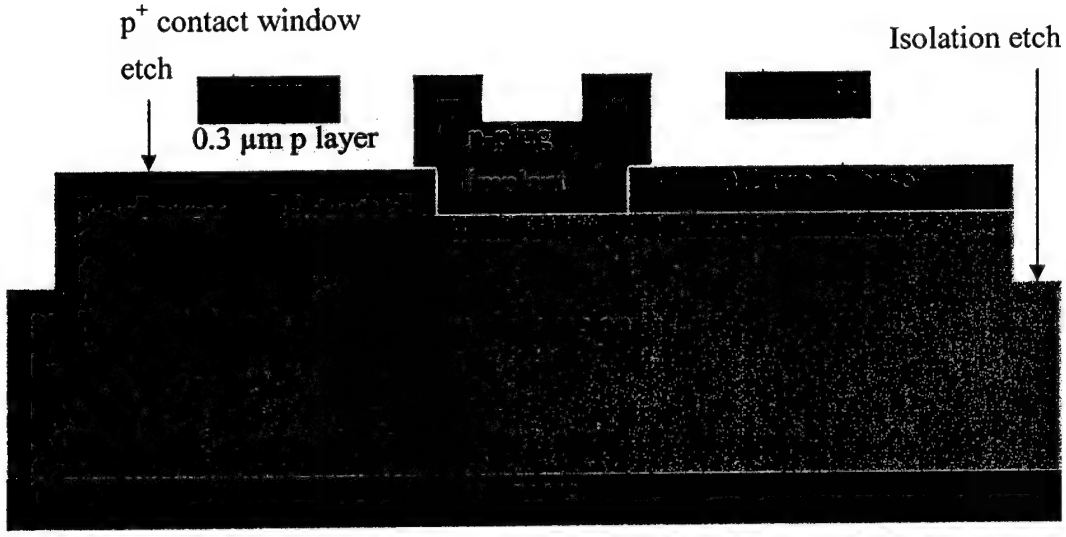


e) After n^- plug implants

Fig. 3.3. Process flow of epiDMOS structures (continued).

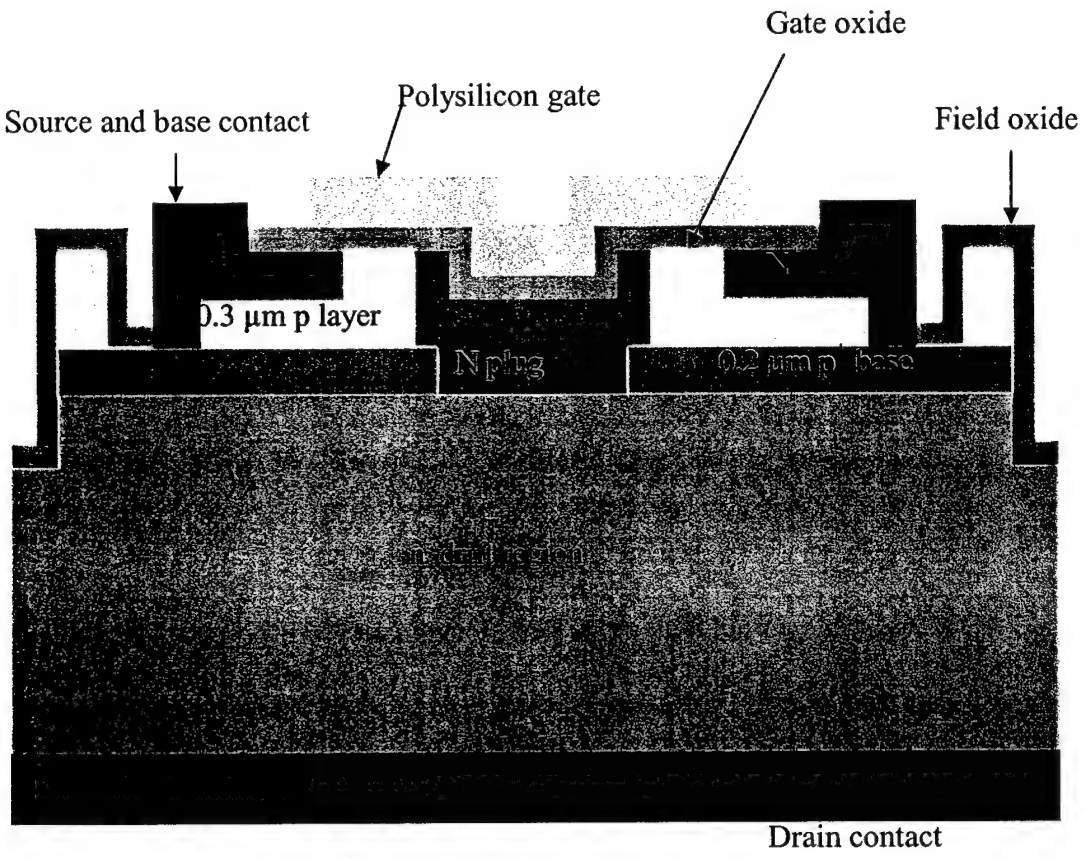


f) After RIE etch of p^+ contact



g) After RIE of isolation etch

Fig. 3.3. Process flow of epiDMOS structures (continued)



h) Final device

Fig. 3.3. Process flow of epiDMOS structures.

3.3 MEDICI Simulation of the Epitaxial Base DMOS Structure

In order to gain a better understanding of the structure and operation, device simulations are performed using TMA (Technology Modeling Association, Inc) MEDICI 2D device simulator [28]. The electrical characterization of the device structure is governed by Poisson's equation:

$$\nabla^2\varphi = -\frac{q}{\varepsilon}\left(p - n + N_D^+ - N_A^-\right) \tag{3.1}$$

and continuity equations:

$$\frac{1}{q}\nabla.\bar{J}_p = U_n \tag{3.2a}$$

$$\frac{1}{q}\nabla.\bar{J}_p = U_p \tag{3.2b}$$

where φ is the electrostatic potential, N_D^+ and N_A^- are the ionized impurity concentrations, J_n and J_p are electron and hole current densities respectively, and U_n and U_p (cm^{-3}/sec) represent net electron and hole recombination respectively. MEDICI solves the above three equations self-consistently for the electrostatic potential and electron (n) and hole (p) concentrations. In this simulation, fixed oxide charge in the oxide and interface charge and traps have not been considered. Carrier transport is modeled by the drift-diffusion equations:

$$\bar{J}_n = q\mu_n n\bar{\xi} + qD_n\nabla n \tag{3.3a}$$

$$\bar{J}_p = q\mu_p p\bar{\xi} - qD_p\nabla p \tag{3.3b}$$

The current densities consist of a drift component caused by the electric field ξ and a diffusion component caused by the concentration gradient. The mobility values (μ_n and μ_p) are given in the next section. The diffusion coefficients (D_n and D_p) are related to mobility by the Einstein equation.

3.3.1 Physical models applied for 4H-SiC

The physical models employed in the simulations include:

1) Mobility model
2) Bandgap and intrinsic carrier concentration
3) Generation-Recombination
4) Impact Ionization
5) Incomplete ionization of impurities

1) Mobility model:

Low field mobility models degradation of mobility due to ionized impurity scattering, phonon scattering, and carrier-carrier scattering. The field dependent mobility model further includes the degradation of mobility due to applied electric fields. To model mobility for electric field in the direction of current flow, the following Caughey-Thomas expression is used [29]:

$$\mu_{n,p} = \frac{\mu_{0n,0p}}{\left[1+\left(\frac{\mu_{0n,0p}\xi_{n,p}}{v_{satn,satp}}\right)^{\beta_{n,p}}\right]^{\frac{1}{\beta_{n,p}}}} \tag{3.4}$$

where μ_{n0} and μ_{p0} are the low field mobilities. In this model the carrier velocities saturate at high electric fields. The necessary parameters for 4H-SiC are given in the following Table 3.1 [6].

Table 3.1

Temperature	Parameter	4H-SiC
300°K	v_{satn}	$2.2 \cdot 10^7$ cm/sec
	β_n	1.2

The low field mobilities (μ_{n0} and μ_{p0}) are calculated from the following Caughey-Thomas expression, which models the combined effect from lattice and ionized impurity scattering. The Caughey-Thomas parameters were found by fitting equation (3.5) to experimentally obtained data [8].

$$\mu_{n,p} = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N_D + N_A}{N_{ref}} \right)^{\gamma}} \tag{3.5}$$

The experimental data calculated is in the direction parallel to the c-axis and at room temperature of 300°K. The mobility model used in the simulation is isotropic in nature, and Table 3.2 includes the necessary parameters [8]:

Table 3.2

Material	μ_{max} (cm^2/V-sec)	μ_{min} (cm^2/V-sec)	N_{ref}	γ
n-4H	947	0.0	$1.94 \cdot 10^{17}$	0.61
p-4H	124	15.9	$1.76 \cdot 10^{19}$	0.34

2) Bandgap and intrinsic carrier concentration:

The intrinsic carrier concentration is calculated from the energy bandgap and from the electron and hole effective density of states using the following relation:

$$n_i = \sqrt{N_c N_v} e^{-\frac{E_g}{2K_B T}} \tag{3.6}$$

A bandgap value E_g of 3.23 eV [30] and the effective density of states in the valence band $N_v = 2.5 \cdot 10^{19}$ cm^{-3} and in the conduction band $N_c = 1.669 \cdot 10^{19}$ cm^{-3} were used [31]. The accurate value of intrinsic carrier concentration is important for high temperature-high power electronics because the amount of leakage current in a reversed biased device depends on this parameter.

3) Generation and recombination:

The Shockley-Read-Hall (SRH) recombination -generation rate assuming mid-gap traps is given by the following relation [32]:

$$U_{SRH} = \frac{np - n_i^2}{\tau_n(n + n_i) + \tau_n(p + n_i)} \tag{3.7}$$

The electron and hole lifetime can be modeled as a function of doping at 300°K with the following relation [32],[33]:

$$\tau_{n,p} = \frac{\tau_{n0,p0}}{1 + \left(\frac{N_D + N_A}{N_{n,p}^{SRH}}\right)^{\gamma_{ns,ps}}} \tag{3.8}$$

4H-SiC is a wide and indirect band gap semiconductor, therefore carrier lifetime is usually long for materials with low defect densities. For a MOSFET, carrier lifetime may not have any significant effect on device performance.

4) Impact ionization:

Impact ionization rate is a very important parameter for calculating the critical electric field and maximum blocking voltage capability of a reverse biased device. In the presence of a high electric field, an electron on the average generates one electron hole pair over a distance $1/\alpha_n$. The ionization rates are modeled according to Selberher [29]:

$$\alpha_n = \alpha_{n,II} \exp\left(-\left(\frac{E_n^{crit}}{E}\right)\right)^{EXN.II} \tag{3.9a}$$

$$\alpha_p = \alpha_{p,II} \exp\left(-\left(\frac{E_p^{crit}}{E}\right)\right)^{EXP.II} \tag{3.9b}$$

The rates have an exponential dependence on the electric field (E) parallel to the direction of current flow. Values for ionization rates and critical electric fields for 4H-SiC material can be found from Konstatinov et al [4]. A photomultiplication technique was employed to determine the ionization rates. The measurement was performed on 0.2mmx0.2mm defect-free diodes. The necessary MEDICI parameters for electrons were extracted by fitting equation (3.9a) to Konstantinov's 4H-SiC data for electrons. The parameters for hole impact ionization coefficient were taken from Raghunathan et al. [34]. P-EBIC (Pulsed electron beam induced current) measurements were performed for extracting the hole ionization rate. The fabricated diodes were less than $5 \cdot 10^{-5}$ cm^2 and were free from micropipes or other dislocation defects. Since real power devices will always have at least some screw dislocation in the active area, the blocking voltage obtained from MEDICI simulation can be slightly optimistic.

5) Incomplete ionization of impurites:

Doping of SiC epitaxial layers is accomplished in situ during the crystal growth of the epilayer. N-type doping is achieved by nitrogen gas flow and for the p-type epilayer TMA (trimethyl alluminum) or B_2H_6 (diborane) gas is flowed. Nitrogen donor atoms mainly occupy the C-sites and Al donor atoms occupy only the Si-lattice sites [35]. Doping is controlled by site-competition epitaxy technique where the Si/C ratio is varied to control the dopant incorporation during epitaxial growth. Doping with nitrogen in 4H-SiC creates two energy levels [36]:

$E_c - E_{D1} = 52$ meV

$E_c - E_{D2} = 91.8$ meV

Deep levels can lead to incomplete ionization of the dopants. Both energy levels contribute equally to the total doping concentration by distributing the dopant atoms in equal number of hexagonal and cubic lattice site (4H-SiC) [37]. MEDICI simulation can use one energy level, and Bakowski et al. [30] provides a single effective donor level at 65 meV. For Al doped 4H-SiC layers, the ionization energy is at $E_A - E_v = 191$ meV (the shallow level).

3.3.2 Design study of the epiDMOSFET structure

The cross-section of the MEDICI simulated epiDMOS structure is shown in Fig. 3.4. The structure consists of a $7 \cdot 10^{15}$ cm^{-3} doping and 10 μm thick drift region on top of a 2 μm thick n^+ substrate (as simulated – the actual substrate is about 300 μm thick). The p-base has a $5 \cdot 10^{16}$ cm^{-3}, 0.3 μm channel epilayer on top of 0.2 μm, $5 \cdot 10^{18}$ cm^{-3} p^+ blocking layer. The n^- plug region that connects the source to the drain was also introduced with a doping of $1 \cdot 10^{17}$ cm^{-3}. 0.3 μm of n-type step coverage over the patterned p^+ region was also assumed. The n^+ source is 0.15 μm deep and $2 \cdot 10^{18}$ cm^{-3} doped. The channel length is the distance between the n^+ source and patterned p^+ epilayer, and is limited by the lithography process. Here, a channel length of 3 μm was used. A gate oxide thickness of 1500^0A was assumed, which represented a uniformly deposited polysilicon oxide. Only half of the device was simulated due to symmetry of the structure. A rectangular mesh was specified consisting of about 3000 nodes of an available 3200. The MEDICI program automatically generates triangular grids by adding diagonals to the rectangular structure. The simulation results are often grid dependent, and the number of grid points directly affects the speed and accuracy of the simulation. For this reason a denser grid was used wherever concentration and electric field changed rapidly such as: the gate oxide on top of the step and n^- plug region; the n^+ source to p-channel junction; the p^+ base-n^- drift region junction, etc. A wider grid step was used in the drift region, as concentration and electric field changed gradually. Once the structure was defined, the proper physical models and material coefficients were also defined.

a) <u>On-state Analysis:</u>

In order to achieve more realistic results, a low-field surface mobility model SRFMOB was also included in the simulation. The model is only applied at the interface, and to model the current flow away from the interface, the empirical mobility model for SiC from the Caughy-Thomas equation described in section 3.3.1 is also used. At the SiO_2/SiC interface, the MEDICI simulation uses the minimum of the SRFMOB and the selected low-field mobility. In the simulations, the channel mobility was varied from 100, 50, to 30 cm^2/Vsec. Figure 3.5 shows the extracted mobility values from the interface to a

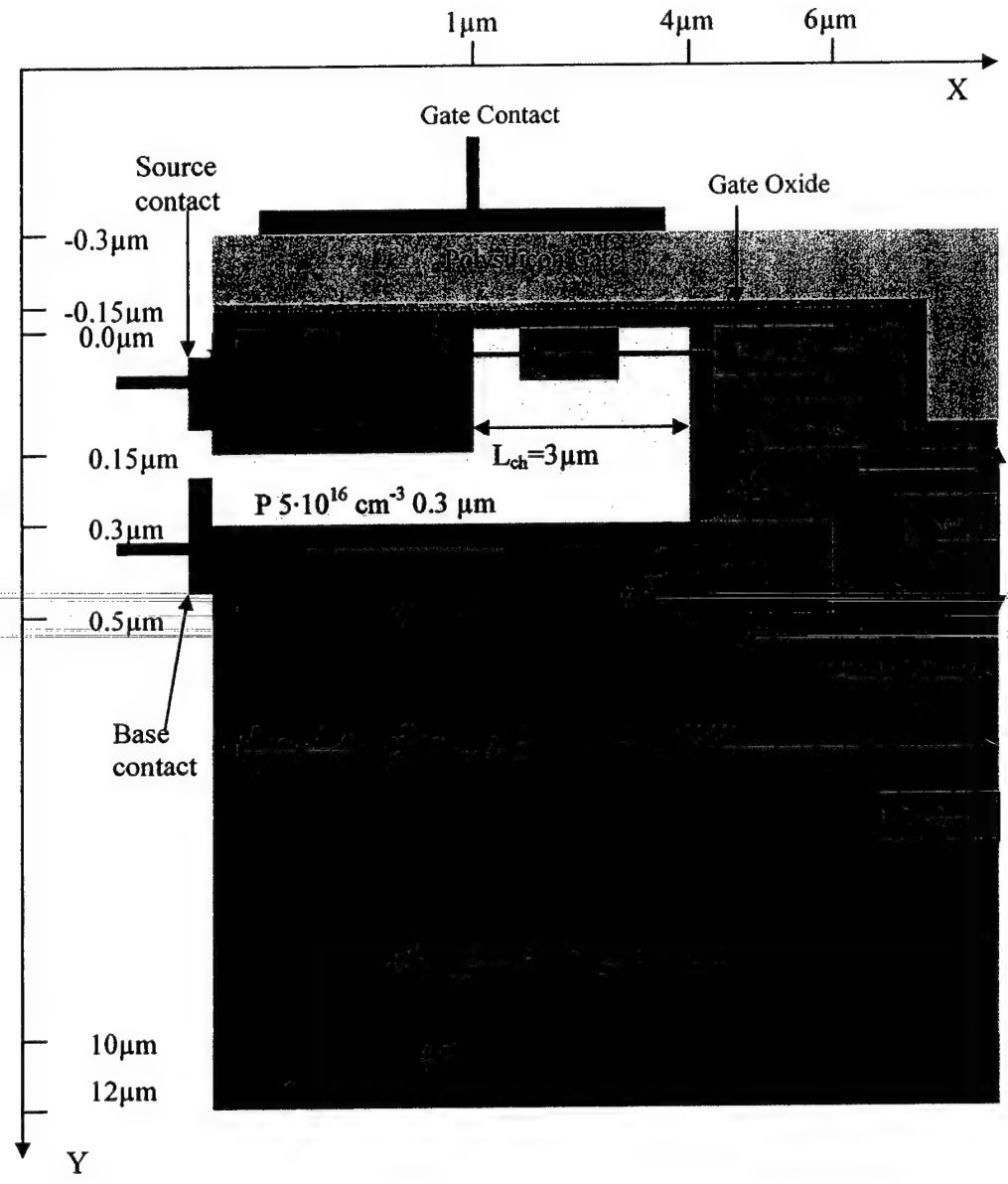


Fig. 3.4. Schematic cross-section of the simulated epiDMOS structure.

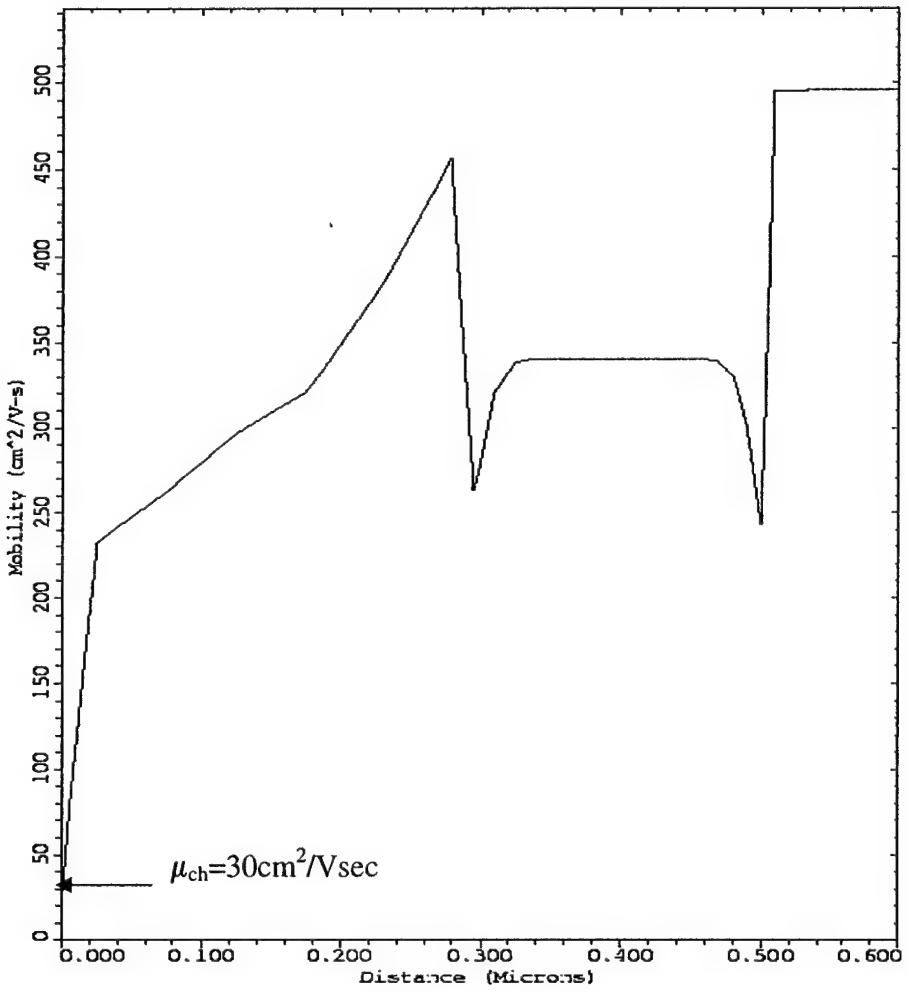


Fig. 3.5. Inversion channel mobility value at the SiC/SiO_2 interface is 30 cm^2/Vsec (at x=3.0μm and y=0.0μm). The mobility value is extracted from the MEDICI simulation at x=3.0μm and y=0.0 to y=0.6μm.

distance of 0.6 μm into the semiconductor for the epiDOMS structure with L_{JFET}=6 μm and the inversion channel mobility limited to 30 cm^2/Vsec at the interface.

The I-V characteristics were simulated by grounding the source and base and by varying the gate and drain voltages. Figure 3.6 shows the current flow lines of the simulated structure. The current flow path consists of: 1) the 3 μm inversion mode MOSFET channel; 2) an accumulation (n-plug overlap) channel of 2 μm; 3) a UMOS vertical accumulation channel of 0.2 μm; 4) a JFET region between two p^+ base; and 5) finally through the 10 μm n^- drift region to the n^+ substrate.

The specific on-resistance is then extracted from the linear region of the simulated drain I_d-V_{ds} characteristics. Figure 3.7 shows the I-V curve for the epiDMOS structure with L_{JFET}=6 μm and a channel mobility of 30 cm^2/Vsec. The specific on-resistance value was then calculated from the drain characteristics of the simulated epiDMOSFET structures with the pitch (6 μm+L_{JFET}/2) varying from 7 to 9 μm as the L_{JFET} varied from 2 to 6μm. In order to allow lengths for realistic fabrication process, the on-resistance values were then re-calculated with a realistic pitch of (10.5 μm+L_{JFET}/2) as shown in Table 3.3.

Table 3.3

R on-specific (mΩ-cm^2)					
L_{JFET} (μm)	2	3	4	5	6
Pitch=10.5+L_{JFET}/2 (μm)	11.5	12	12.5	13	13.5
μ_{ch}=30 (cm^2/Vsec)	17.94	17.66	18.31	16.99	19.5
50 (cm^2/Vsec)	12.88	12.96	12.91	12.8	12.66
100 (cm^2/Vsec)	9.64	8.8	8.39	7.39	8.175
$\mu_{ch}\rightarrow\infty$($cm^2$/Vsec)	$R_{JFET,sp}$+ $R_{Drift,sp}$ (mΩ-cm^2)				
	5.95	5.155	4.25	3.82	3.16

The JFET resistance decreases as the L_{JFET} gap increases, however the specific on-resistance can increase as the area of the device is increased. This trend in $R_{on,sp}$ is observed for μ_{ch}=100 cm^2/Vsec. For μ_{ch}=30 and 50 cm^2/Vsec, there is some deviation in data. The drift and JFET resistance do not depend on inversion channel mobility, and JFET resistance decreases as the L_{JFET} gap increases. The channel resistance (R_{ch}), the

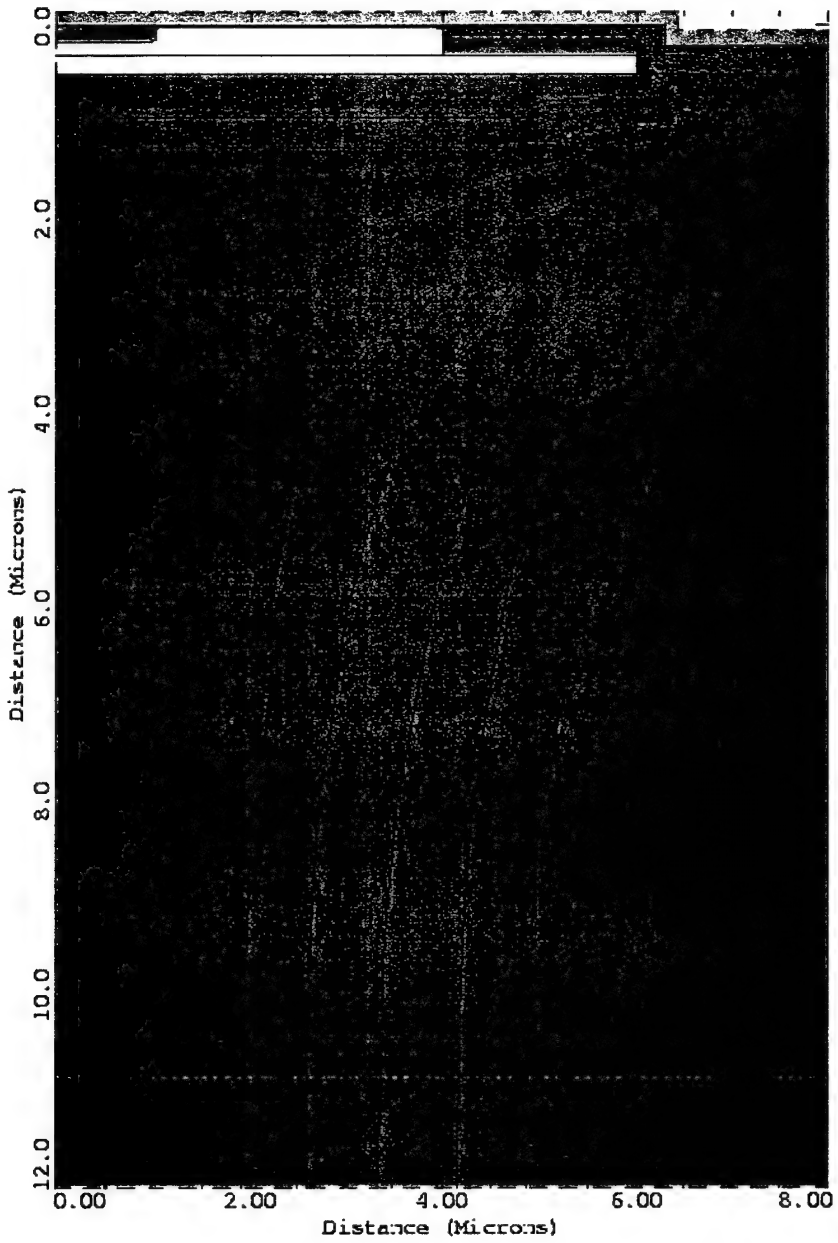


Fig. 3.6. Current flow lines of epiDMOS structure at V_{gs}=30V and V_{ds}=1V.

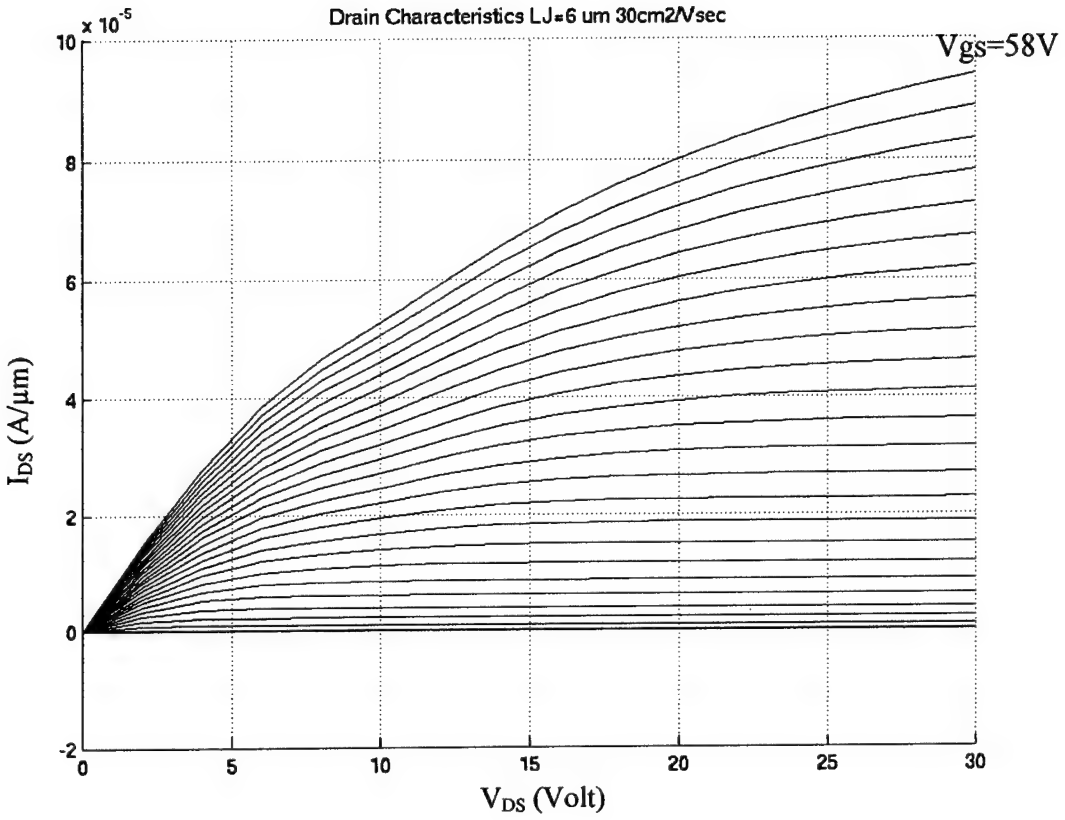


Fig. 3.7. I-V characteristics of epiDMOSFET with L_J=6.0μm and μ_{ch}=30 cm^2/Vsec The gate voltage was varied from 0 to 58V at 1V step and the drain voltage was varied from 0 to 30V.

resistance from the n-plug ($R_{n\text{-}Plug}$), and from the UMOS channel (R_{UMOS}) depend on the channel mobility, and decreases as the mobility value increases. The picth of the MOSFET, which is also a factor in the specific on-resistance, increases as L_{JFET} increases.

Figure 3.8 shows the extrapolation of $R_{on\text{-}specific}$ vs. 1/mobility curve. As channel mobility goes to ∞, the y-intercepts of the L_{JFET} =2,3,4,5 and 6 μm curve give the specific on-resistances of R_{JFET} plus R_{drift} only, as the R_{ch}, R_{UMOS}, and $R_{n\text{-}plug}$ resistances go to zero. Here no source or base contact resistance was included. With $\mu_{ch} \rightarrow \infty$ the effect of R_{JFET} can be seen as the L_{JFET} is decreased (see also Table 3.3). The channel resistance is dominating, even with a reasonable mobility value of 30 cm^2/Vsec, and is between 18-20 mΩ-cm^2. For a realistic cell pitch S=13.5 μm and with a L_{JFET}=6 μm, from the extrapolation of the $R_{on\text{-}specific}$ vs. 1/mobility curve we find $R_{JFET,sp}+R_{Drift,sp}$=3.2 mΩ-cm^2. The channel specific on-resistance, $R_{ch,sp}$, for a μ_{ch}=30 cm^2/Vsec, L_{ch}=3 μm and E_{ox}=3.87 MV/cm (Vgate=58V, t_{ox}=1500^{0}A) is then calculated to be 10.11 mΩ-cm^2. So, from the total $R_{on,sp}$=19.5 mΩ-cm^2, the $R_{n\text{-}plug,sp}+R_{UMOS,sp}$=6.2 mΩ-$cm^2$. Thus, from MEDICI simulations we find that the drain plug is also acting like a channel resistive path and is not helping at all! The minimum channel length that can be used is L_{ch}=3 μm (inversion channel)+2.3 μm (drain plug overlap)+0.2 μm (UMOS accumulation channel)=5.5 μm. Thus the epiDMOS version limits us with a high cell pitch, since we have to allow lengths for realistic fabrication processes.

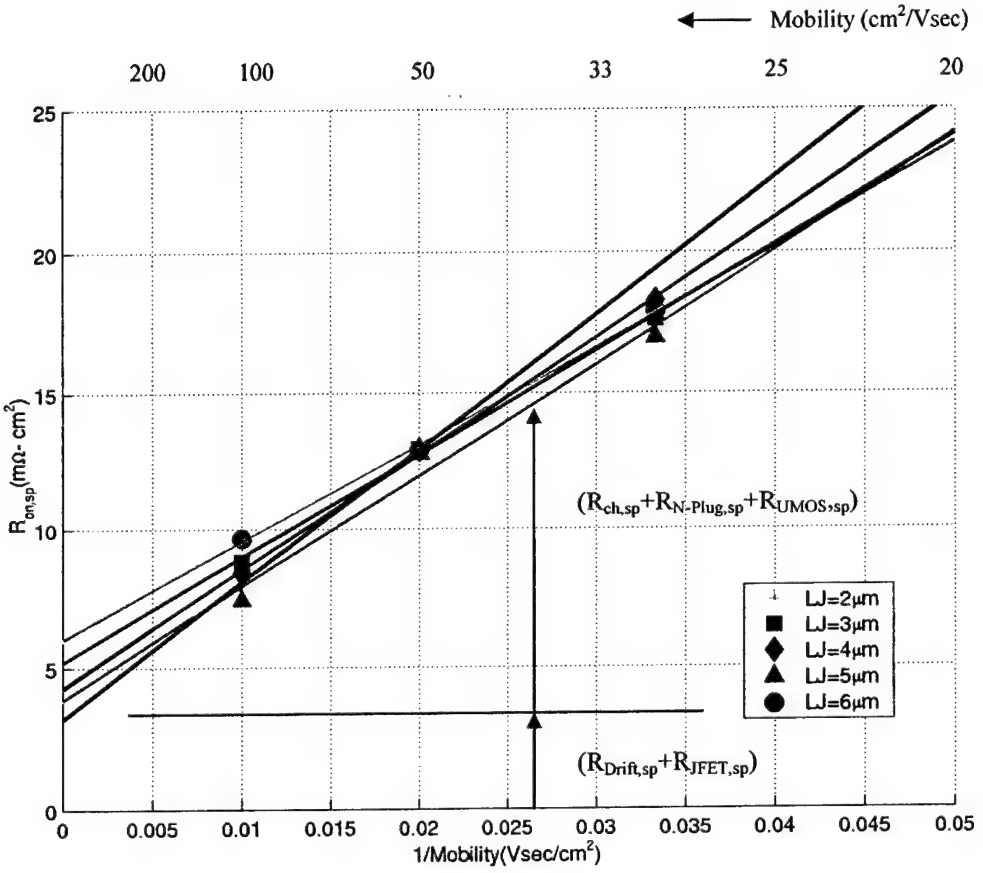


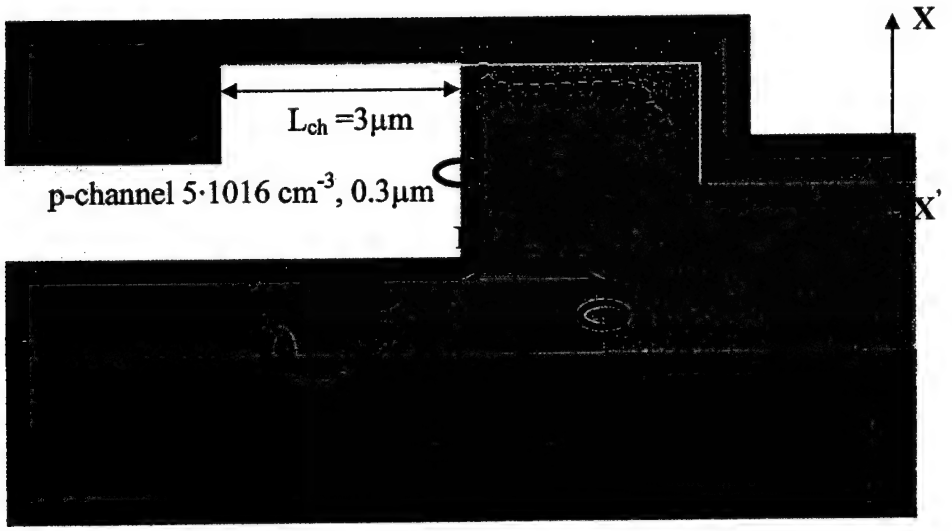
Fig. 3.8. Extrapolation of the MEDICI results from the simulated epiDMOS structure. The $(R_{Drift,sp}+R_{JFET,sp})$ resistance does not depend on channel mobility, and are extracted at $\mu_{ch}\rightarrow\infty$. Any additional increase in the total $R_{on,sp}$ is due to the combination of $(R_{ch,sp}+R_{nplug,sp}+R_{JFET,sp})$, as shown in figure.

b) Off-state Analysis:

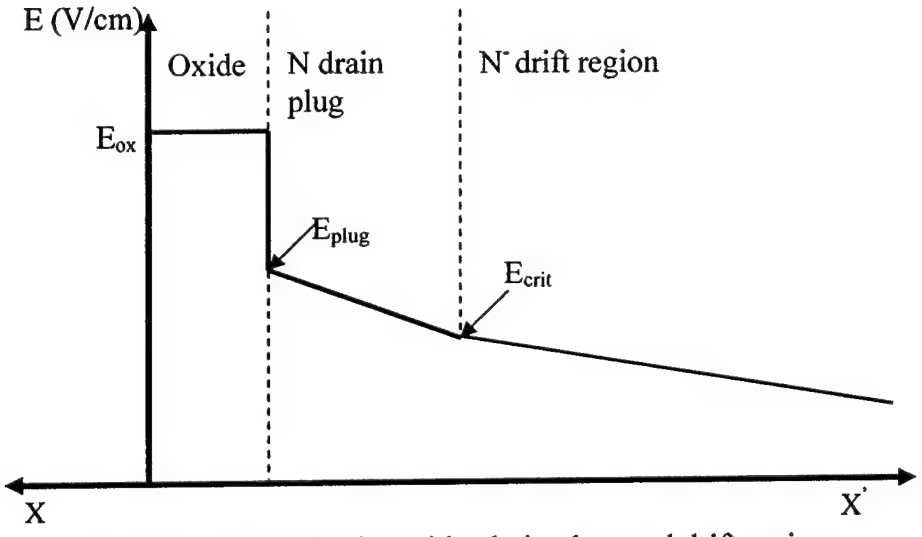
In order to make a connection from the channel to the drain, an n-type drain plug region is necessary for the epiDMOSFET structures. The doping of the n-type plug region needs to be high enough to compensate the p-channel doping and provide an n-type connection to the drain, and also to prevent pinch off of the channel region from the heavily doped p^+ base region, as shown in Figure 3.9. On the other hand, it should be low enough to limit the field in the oxide at a reliable value of $\leq$ 4 MV/cm. During the blocking state, when the electric field in the n^- drift region reaches its critical value of 2.1 MV/cm (for a doping of $7.0 \cdot 10^{15}$ cm^{-3}); the field in the n-plug region is 2.65 MV/cm ($\Delta E = qN_D t_{nplug}/\varepsilon_{SiC} = 0.55$ MV/cm). The field in the oxide is 6.67 MV/cm ($E_{ox} = E_{plug}\varepsilon_{SiC}/\varepsilon_{ox}$)! So, the oxide is under high field stress as the avalanche condition is reached in the semiconductor. During the on-state, with $1 \cdot 10^{17}$ cm^{-3} plug doping and with 1V reverse bias applied to the base (due to the voltage drop across the MOSFET channel), the plug region is almost totally depleted from the p^+ base (0.21 μm), and the current flow is through the accumulation layer only (plug overlap). As the plug doping is increased to $3 \cdot 10^{17}$ cm^{-3}, the depletion region extension decreases to 0.12 μm, but the stress in the oxide is increased further. In order to avoid premature oxide breakdown and for reliable stable operation, the drop in field in the n-plug region should be kept below 0.55 MV/cm. Table 3.4 summarizes the calculations of field in the oxide and the depletion region extension from the heavily doped p^+ base to the n-drain plug region.

Table 3.4

N-plug doping (cm^{-3})	E_{ox} (MV/cm)	Built in potential (Volt) $V_{bi} = \frac{kT}{q}\ln\frac{N_A N_D}{n_i^2}$	Depletion from p^+ base (μm) $X_{depl(nplug)} \approx \sqrt{\frac{2\varepsilon_s \phi_s}{qN_D}}$
$1 \cdot 10^{17}$	6.67	3.056 V	0.21 μm
$3 \cdot 10^{17}$	9.45	3.084 V	0.12 μm



a) Simulated epiDMOS structure



b) Electric fields in the oxide, drain plug, and drift region

Fig. 3.9 a) Depletion region (red dotted line) extension from p^+ base region and b) Electric field calculation in the oxide and drain plug region along cross section X-X'.

In the off-state (blocking mode) the source, p^+-base and gate were grounded and a positive voltage was applied to the drain. The maximum electric field at the SiO_2/SiC interface ($E_{ox,max}$) and the electric fields at the p^+ base-n-plug (pn#1) junction, at the p-channel –n-plug (pn#2) junction, and at the p^+ base- n^- drift region (pn#3) junction were then extracted from the MEDICI simulations with an applied voltage of 1200 volts and with an n-plug doping of $1 \cdot 10^{17}$ cm^{-3}. Table 3.5 summarizes all the results extracted from the MEDICI simulations. Figure 3.10 shows 3D-electric field plot, where $E_{ox,.max}$=6.78 MV/cm when the n-plug doping is increased to $3 \cdot 10^{17}$ cm^{-3}. Thus with the epiDMOS design, the applied voltage is limited to only 1200 volts with $1 \cdot 10^{17}$ cm^{-3} plug doping, as the peak field in the gate oxide is under 4 MV/cm for $L_{JFET} \leq 3$ μm.

Table 3.5

L_{JFET} (μm)	Applied Voltage (Volts)	Drain plug doping (cm^{-3})	E_{max} (Oxide) (MV/cm)	E_{max} (PN#1) (MV/cm)	E_{max} (PN#2) (MV/cm)	E_{max} (PN#3) (MV/cm)
2	1200	$1 \cdot 10^{17}$	3.2	2.3	0.275	1.85
3	1200	$1 \cdot 10^{17}$	3.96	2.4	0.275	1.85
4	1200	$1 \cdot 10^{17}$	4.45	2.5	0.27	1.85
	1400	$1 \cdot 10^{17}$	4.78	2.78	0.27	2.05
	1200	$3 \cdot 10^{17}$	6.78	4.4	0.275	1.98
5	1200	$1 \cdot 10^{17}$	4.72	2.63	0.275	1.86
6	1200	$1 \cdot 10^{17}$	4.91	2.64	0.275	1.87
$E_{critical}$ or $E_{ox,max}$ (MV/cm)			4.0	3.05	2.8	2.3

In the epiDMOS design, the n-type drain plug is acting like a resistance added to the channel resistance. Insufficient activation of the n-plug region and extremely low inversion channel mobility can therefore result in a very high specific on-resistance value. This device design is also limited to only 1400 volts (for $E_{ox} \leq 5$ MV/cm, LJ≤4 μm) in the off-state for a 10 μm drift region thickness.

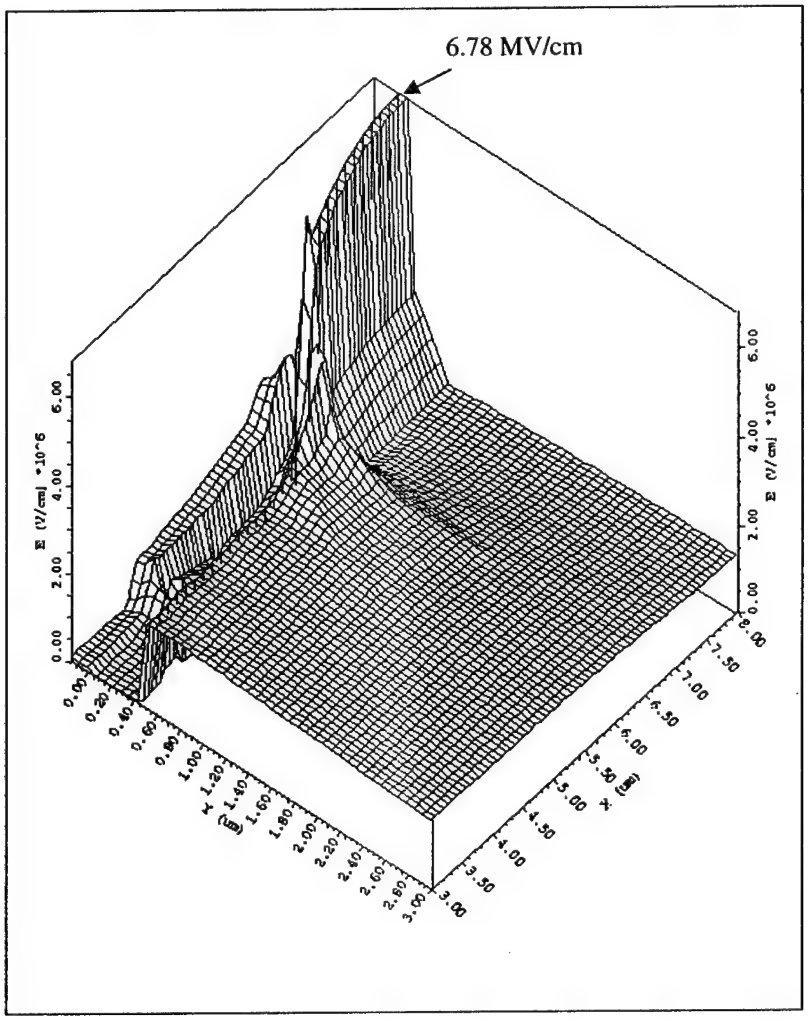


Fig. 3.10. 3D electric field plot for L_{JFET}=4 μm and n-drain plug doping of $3 \cdot 10^{17}$ cm^{-3}.

3.3.3 MEDICI simulation of the EpiAFET structure

1) On-state Analysis:

In the etched epitaxial base accumulation channel DMOS (epiAFET) structure, the p-type channel epi is replaced by an n-type epigrowth. This eliminates the n-type drain plug implantation which was required in the epiDMOS structure. Thus the channel length is almost halved and the $R_{on,sp}$ is also expected to go down by half. Figure 3.11 shows the cross-section of the simulated epiAFET structure. Here, the pitch is $S=8.5+L_{JFET}/2$ with the L_{JFET} length varied from 2 to 6 μm. This design still requires the etching of 0.3 μm n-type epilayer in order to make contact to the p^+ base region. In order to make the pitch smaller, small contact windows can be etched through the same contact window for the source region. Here, the inversion channel is eliminated and the accumulation channel length is only 3.5 μm. In order to lower the stress in the oxide during the off-state, an n-type channel doping of $5 \cdot 10^{16}$ cm^{-3} was used in the simulations.

Figure 3.12 shows the current flow path of the simulated epiAFET structure. The red dotted lines show the depletion boundary. Here, because the n-epilayer doping was lowered in order to reduce the electric field in the oxide, the depletion region from the p^+ base extends further into the n- epilayer. The current flows from the source, through the n-type accumulation channel, between the JFET regions, and finally through the n-type drain region into the n^+ substrate.

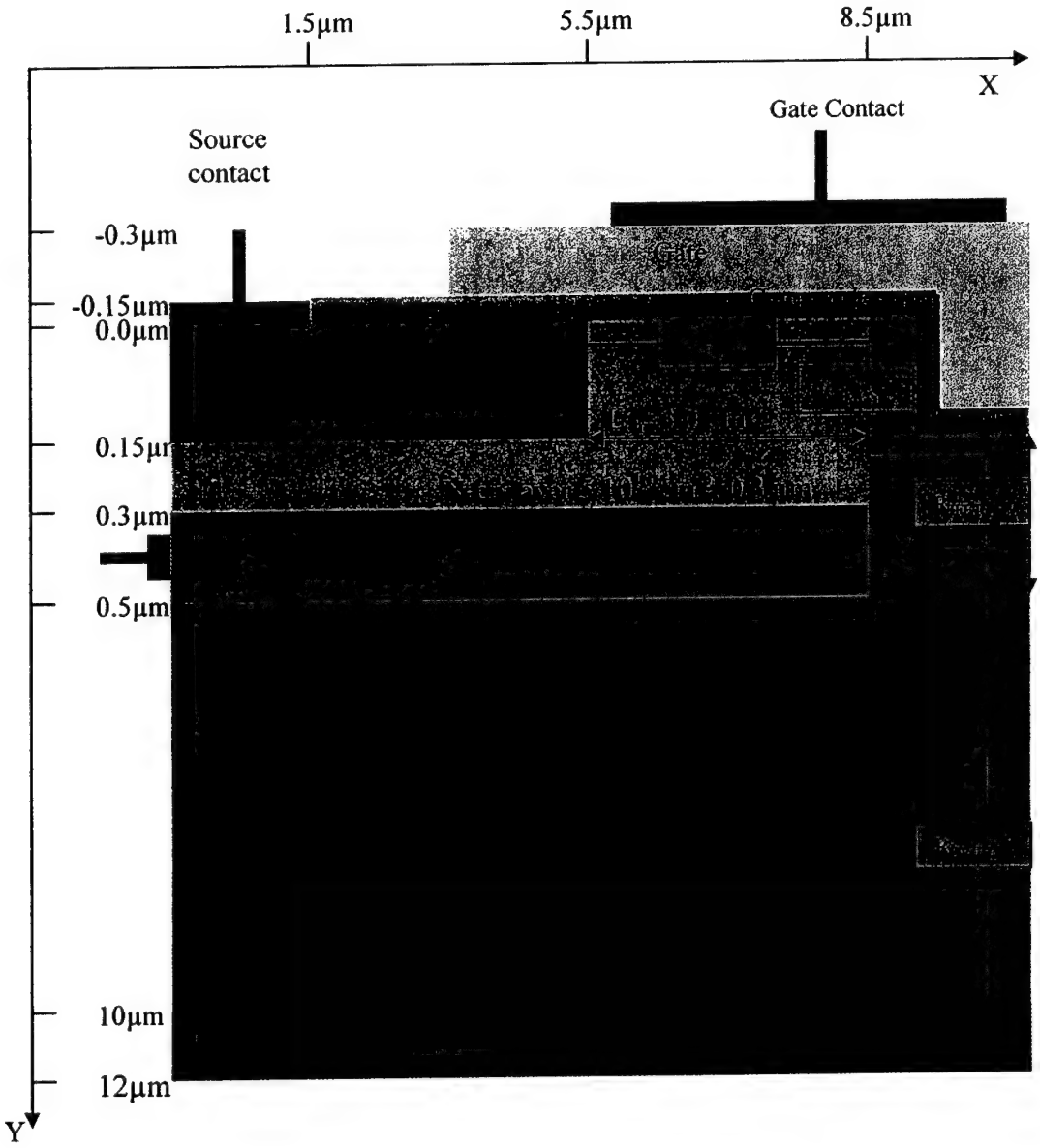


Fig. 3.11. Schematic cross-section of the simulated epiAFET structure

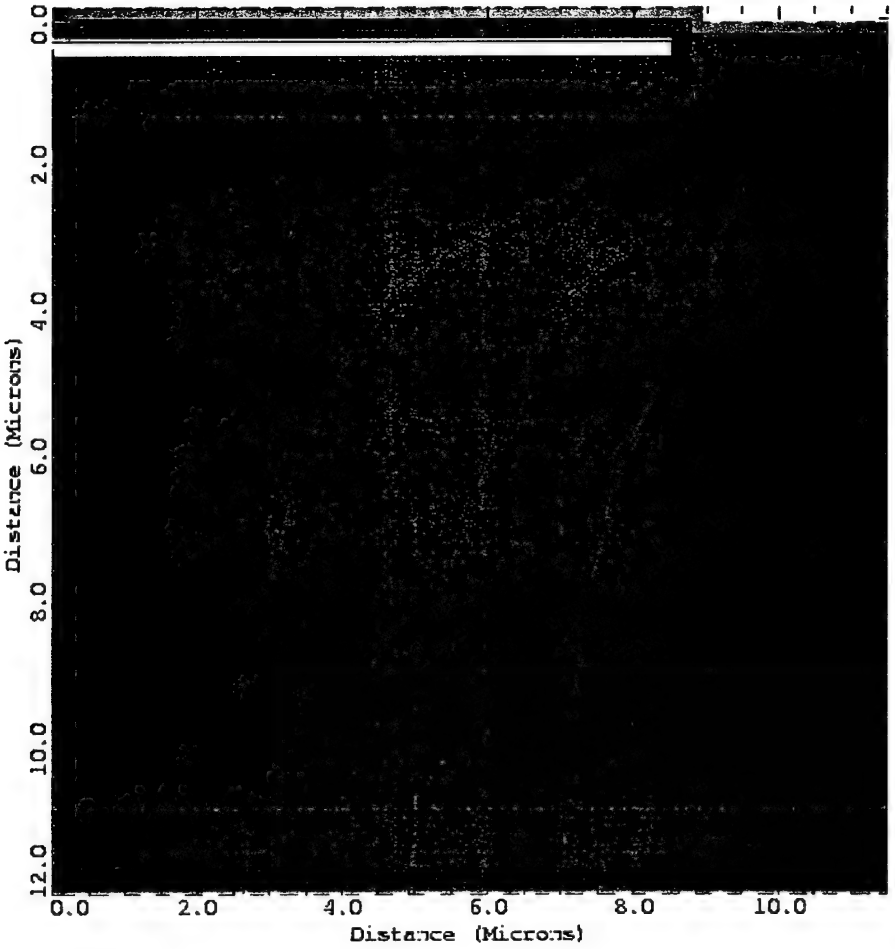


Fig. 3.12. Current flow lines of the simulated epiAFET structure with L_{JFET}=6 μm and μ_{ch}=30 cm^2/Vsec with V_{gs}=2 V and V_{ds}=1 V.

Figure 3.13 shows the I-V curve for the epiAFET structure with L_{JFET}=6μm and μ_{ch}=30 cm^2/Vsec. Table 3.6 summarizes the extracted specific on-resistance values from the linear region of the simulated I-V plots. The $R_{JFET,sp}$+$R_{Drift,sp}$ values were then extracted from the extrapolation of $R_{on,sp}$ vs. 1/mobility curve (Figure 3.14), letting $\mu_{ch}\rightarrow\infty$. The y-intercept of the L_{JFET}=2, 3, 4, 5, and 6 μm curves give $R_{JFET,sp}$+ $R_{Drift,sp}$ which is shown in Table 3.6.

Table 3.6

$R_{on\text{-}specific}$ (mΩ-cm^2)					
L_{JFET} (μm)	2	3	4	5	6
Pitch=8.5+L_{JFET}/2 (μm)	9.5	10	10.5	11	11.5
μ_{ch}=30 (cm^2/Vsec)	8.4	7.95	7.97	8.1	8.26
50 (cm^2/Vsec)	7.38	6.84	6.78	6.89	6.99
100 (cm^2/Vsec)	6.223	5.53	5.42	5.43	5.46
$\mu_{ch}\rightarrow\infty$ (cm^2/Vsec)	$R_{JFET,sp}$ + $R_{drift,sp}$ (mΩ-cm^2)				
	5.38	4.61	4.44	4.42	4.439

The specific on-resistance with a channel mobility of μ_{ch}=30 cm^2/Vsec for L_{JFET}=2, 3, 4, 5 and 6 μm length varies between 8.26-8.4 mΩ-cm^2. The specific on-resistance decreases as the JFET resistance decreases with the increase in L_{JFET} gap, and then increases as the area of the structure increases with the increase in L_{JFET} length.

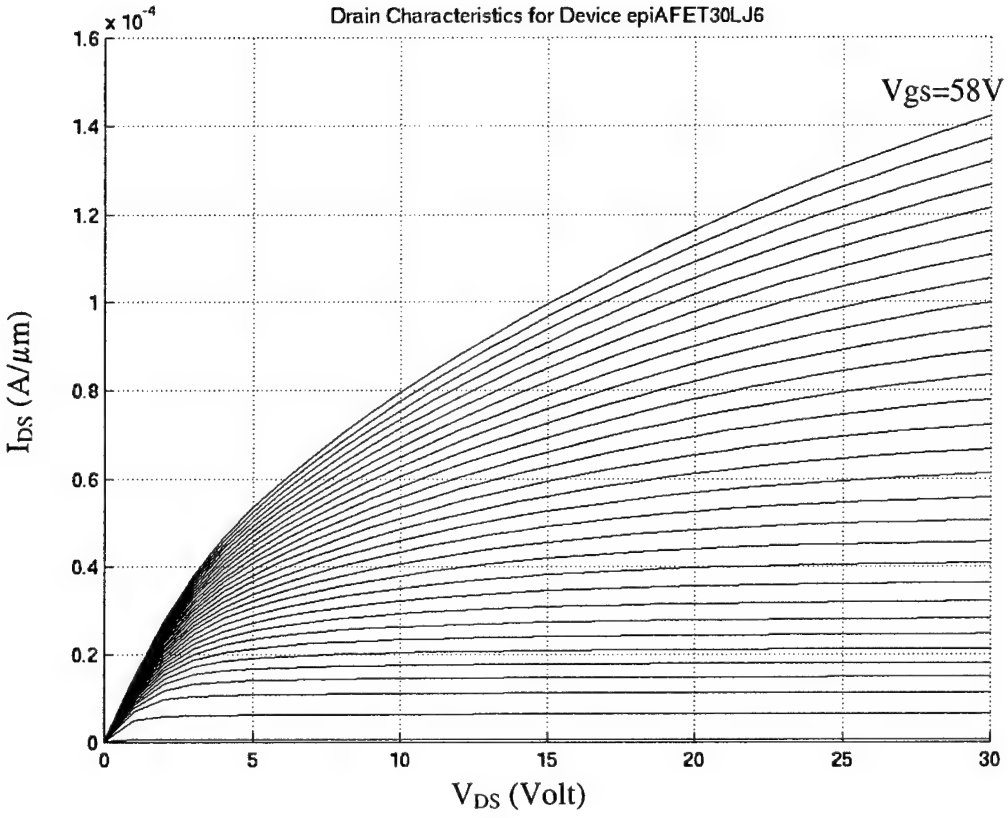


Fig. 3.13. Drain characteristics of a L_{JFET}=6 μm epiAFET structure with μ_{ch}=30 cm^2/Vsec. The gate voltage was varied from 0 to 58 V at 1 V step and the drain voltage varied from 0 to 30 V.

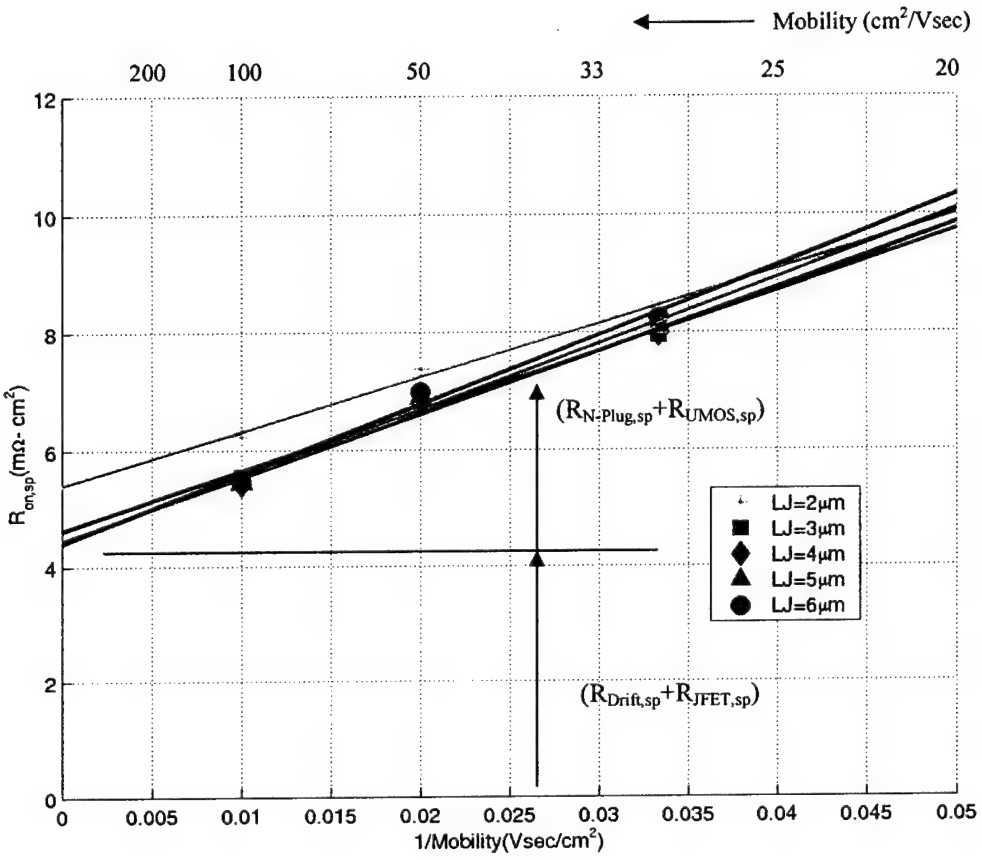


Fig. 3.14. Extrapolation of the MEDICI results from the simulated epiAFET structure. The $(R_{Drift,sp}+R_{JFET,sp})$ resistance does not depend on channel mobility and is extracted at $\mu_{ch}\rightarrow\infty$. Any additional increase in the total $R_{on,sp}$ is due to the combination of $(R_{nplug,sp}+R_{JFET,sp})$, as shown in figure.

2) Off-state Analysis:

The off-state MEDICI simulations were performed by applying 1200 and 1400 volts to the drain with source, base, and gate grounded. The peak field in the oxide was then extracted for L_{JFET}=2, 3, 4, 5 and 6 μm epiAFET structures. Table 3.7 summarizes all the MEDICI simulations performed. From the simulations we find that for a L_{JFET} length of 4 μm, with an applied voltage of 1400 volts, the field in the oxide can be kept close to 4 MV/cm.

Table 3.7

L_{JFET} (μm)	Pitch (μm) $8.5 + L_{JFET}/2$	Doping of the ACCUFET n-type Epilayer (cm^{-3})	Maximum Field in the oxide at 1200V $E_{ox,max}$ (MV/cm)	Maximum Field in the oxide at 1400V $E_{ox,max}$ (MV/cm)
2	9.5	$5 \cdot 10^{16}$	2.82	3.075
3	10	$5 \cdot 10^{16}$	3.5	3.84
4	10.5	$5 \cdot 10^{16}$	3.93	4.28
5	11	$5 \cdot 10^{16}$	4.2	4.58
6	11.5	$5 \cdot 10^{16}$	4.38	4.76

With the epiAFET design structure, the total specific on-resistance can be lowered by a factor of two compared to the epiDMOS design. In both device designs the channel length is limited by the available optical lithography process. They do not require any p-type implantations, and therefore the overall process temperature is limited to 1200^0C. Comparing the epiAFET structure with the best reported power UMOSACCUFET by Tan et al. of Purdue University [11] with a $R_{on,sp}$=15.7 mΩ-cm^2, a 1400 volt blocking voltage and $V_B^2/R_{on,sp}$=125 MW/cm^2, there is a factor of 15.7/7.97=1.97 improvement on the specific on-resistance, but the structure is still limited in the blocking state to 1400 volts for a 10 μm drift layer thickness.

3.4 Etched Epitaxial Base DMOS (epiDMOS) Device Fabrication

The motivation for fabricating the epiDMOSFETs in 4H-SiC is to significantly improve the inversion channel mobility value with an epitaxially grown p-type channel region, thus avoiding any high temperature processing steps above 1200^0C, and simultaneously block high voltages during the off state with the patterned p^+ base regions. The starting material is a heavily doped n^+ substrate with 6H-10 μm, 4H-50 μm, and 4H-100 μm thick n^- epi layers having specific doping concentrations of $3.1 \cdot 10^{15}$ cm^{-3}, $1.1 \cdot 10^{15}$ cm^{-3} and $7 \cdot 10^{14}$ cm^{-3} respectively. The devices were fabricated on quarter pieces of a 25 mm wafer. The 0.2 μm and $5 \cdot 10^{18}$ cm^{-3} doped p^+ base grown by Cree was then carefully patterned by RIE. Figures 3.15a) and b) show sample photographs after the p^+ epigrowth and patterning, and c) is the device cross section at this point.

The p-type channel epilayer with $5 \cdot 10^{16}$ cm^{-3} doping and 0.3 μm thickness was grown after the p^+ epilayer was patterned. Figure 3.16 shows photographs of a) a 4H-10 μm, and b) a 6H-10 μm sample after the p-type channel epigrowth. Figure 3.16c) shows the resulting tapered p channel epilayer on a patterned device (6H-10 μm) with device cross-section. In SiC, the epitaxial growth is performed by a step-controlled epitaxy technique where 4H- and 6H- wafers are routinely off-cut from the basal (0001) plane at an angle of 8° and 3.5° respectively [16]. The resulting steps on the surface contain information of the respective polytype stacking sequence. The growth takes place at these steps, as shown in Fig. 3.17. If the edge of an etched pattern lies perpendicular to the direction of step flow growth or major wafer flat, then that side will have a tapered epi with a thickness of approximately seven times the expected epi thickness for 4H-SiC, as shown in the figure. This tapered problem in the channel region can be avoided if the features are oriented at a 45° angle with wafer flat, as shown in Fig. 3.17d.

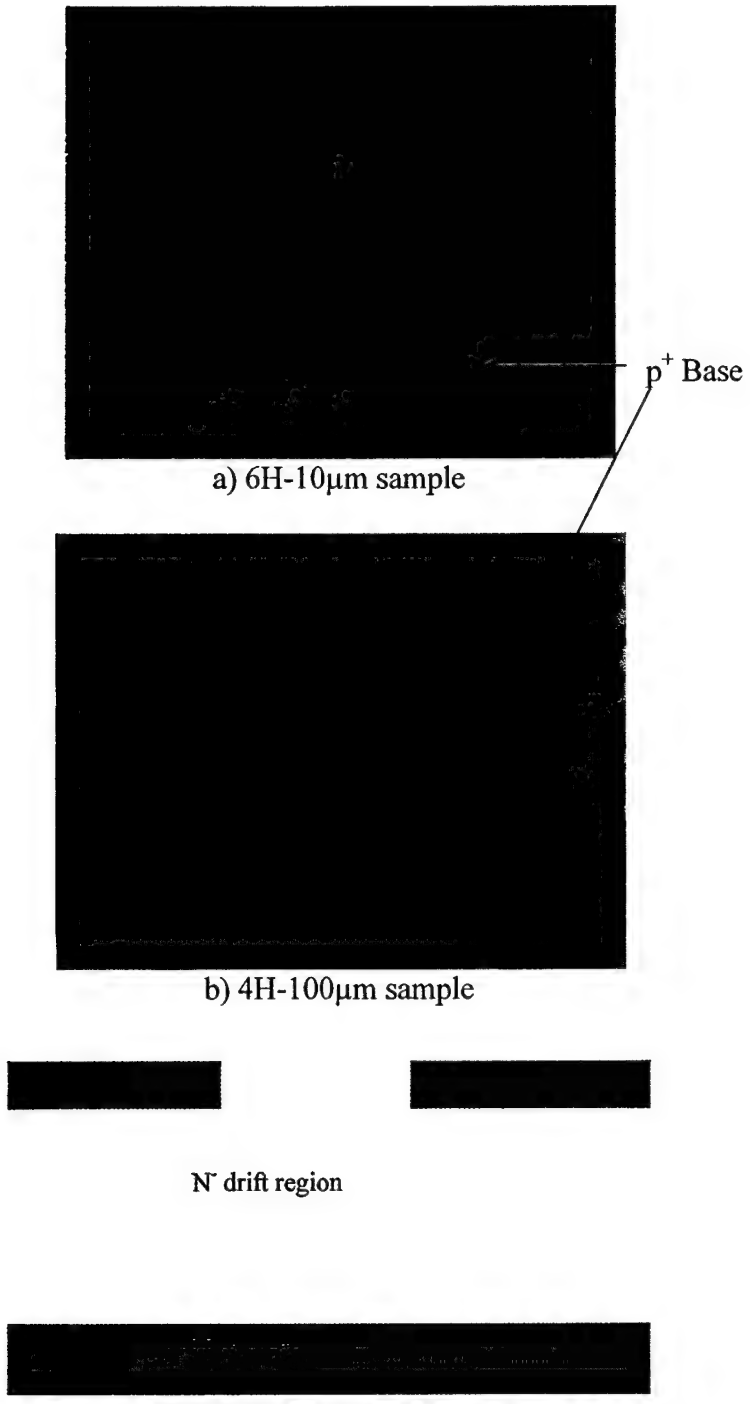
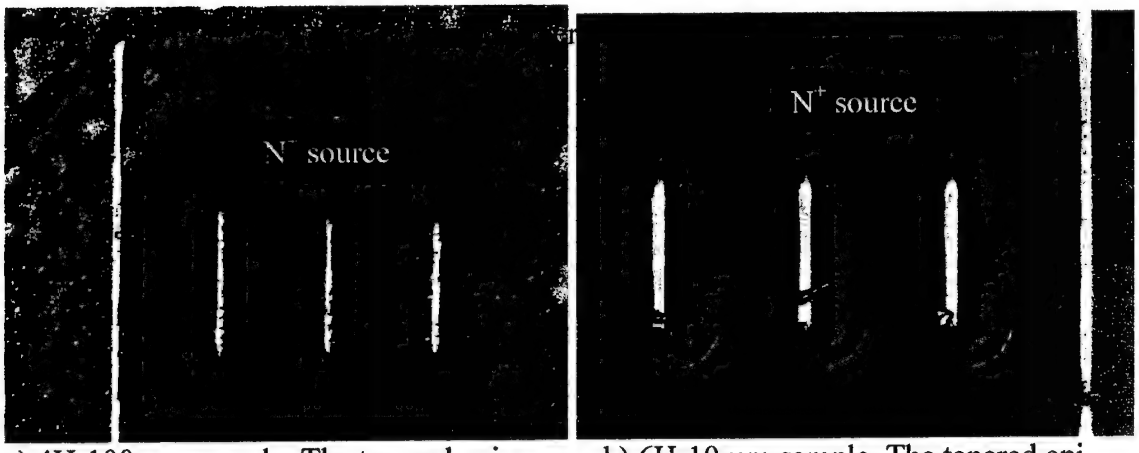
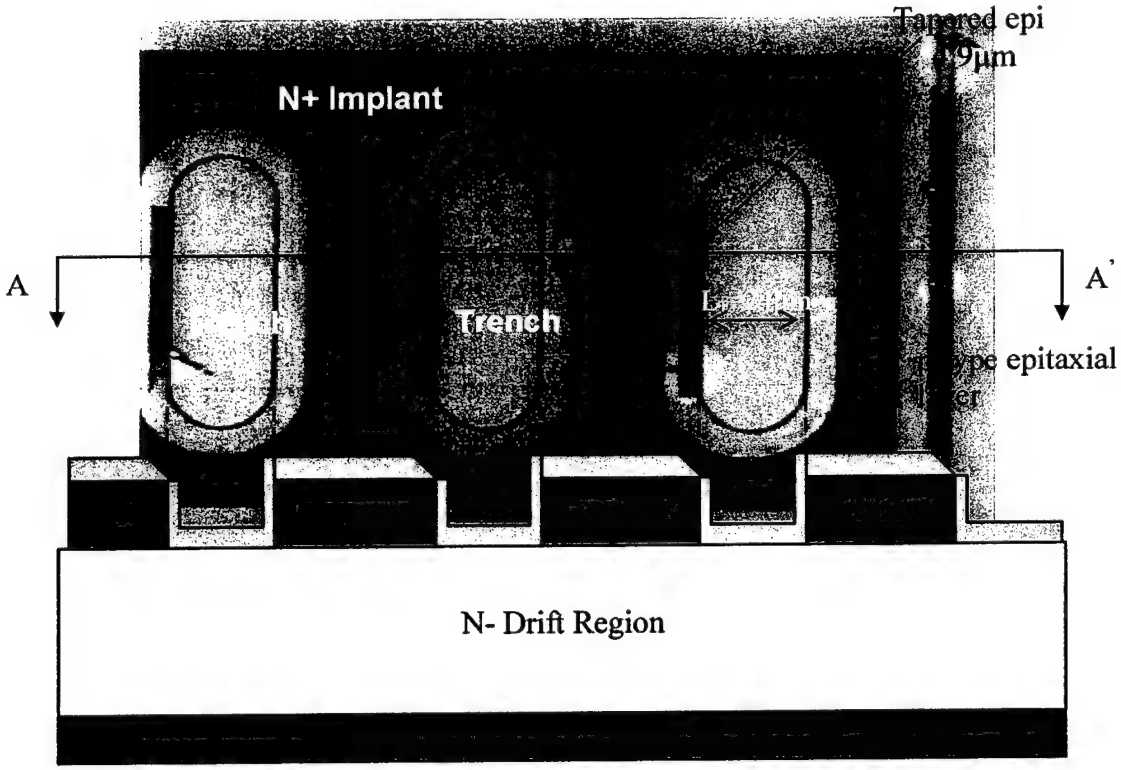


Fig. 3.15. a) 6H-10μm, and b) 4H-100μm sample microphotographs after the p^+ base patterning by RIE, and c) the sample cross-section after the p^+ base patterning.



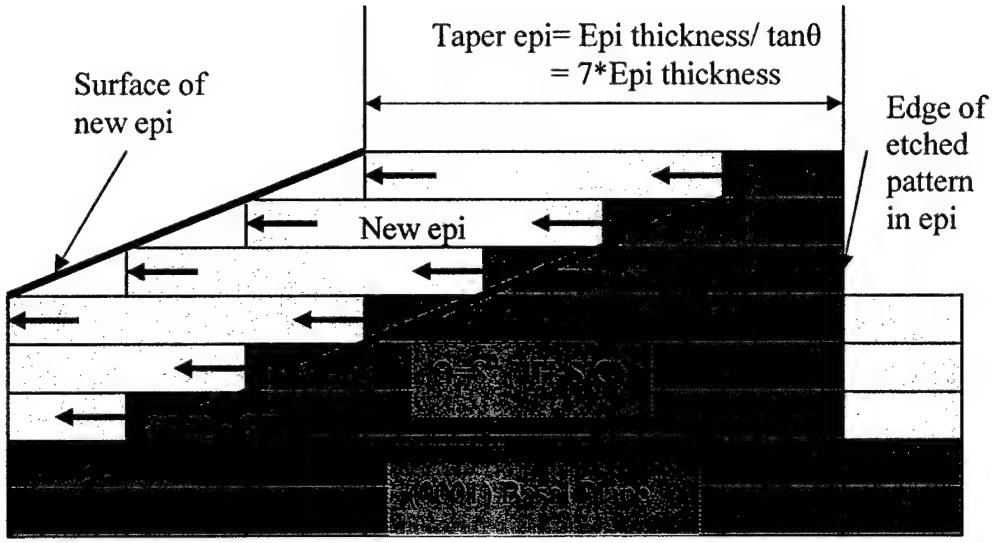
a) 4H-100 μm sample. The tapered epi is approximately 2 μm.

b) 6H-10 μm sample. The tapered epi is approximately 4.8 μm.

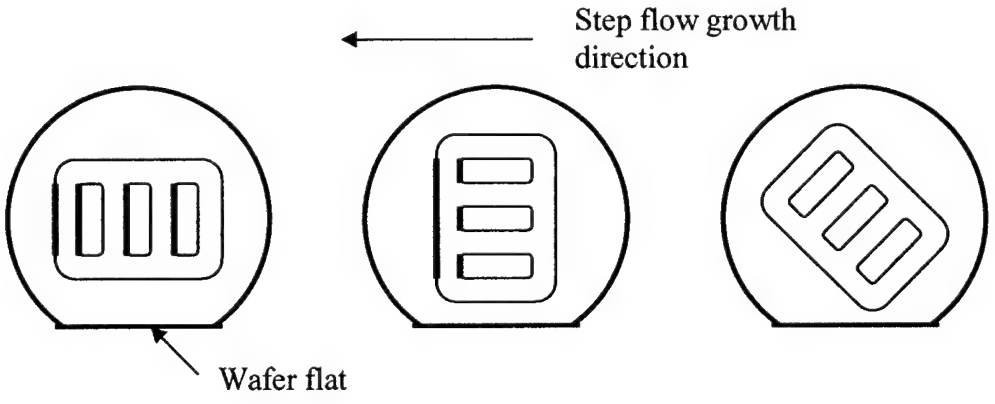


c) sample cross-section after the p-type channel epigrowth

Fig. 3.16. a) 4H-100 μm, and b) 6H-10 μm sample after p-type channel epigrowth over the etched p^+ base regions, and c) device cross-section showing the tapered epilayer problem in the 6H-10 μm sample.



a) Step controlled epitaxy in 4H-SiC



b) c) d)

Fig. 3.17. Step flow growth in SiC material.

The n^+ source implantation was performed by implanting phosphorus into SiC with the dose and energy stated in Table 3.7. The peak concentration is around $2 \cdot 10^{20} cm^{-3}$ and the expected depth is 0.16 μm.

Table 3.7

Implant Species	Phosphorus
Temperature	650°C
Total dose (cm^2)	$1.8 \cdot 10^{15}$
Energy (keV)	Dose (cm^2)
30	$0.6 \cdot 10^{15}$
100	$1.2 \cdot 10^{15}$

The drain plug implantation, which connects the channel to the drain, was performed by implanting nitrogen (see Fig. 3.18 and Fig. 3.19). The implanted energy and dose is given in Table 3.8.

Table 3.8

Implant Species	Nitrogen
Temperature	650°C
Total dose (cm^2)	1.0·13
Energy (keV)	Dose (cm^2)
25	$1.0 \cdot 10^{12}$
70	$1.5 \cdot 10^{12}$
130	$2.0 \cdot 10^{12}$
200	$2.5 \cdot 10^{12}$
280	$3.0 \cdot 10^{12}$

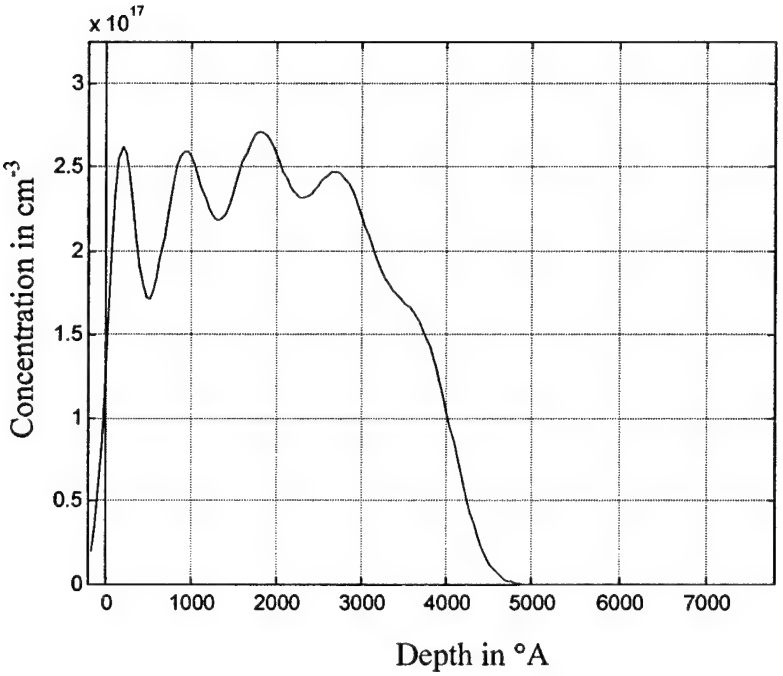
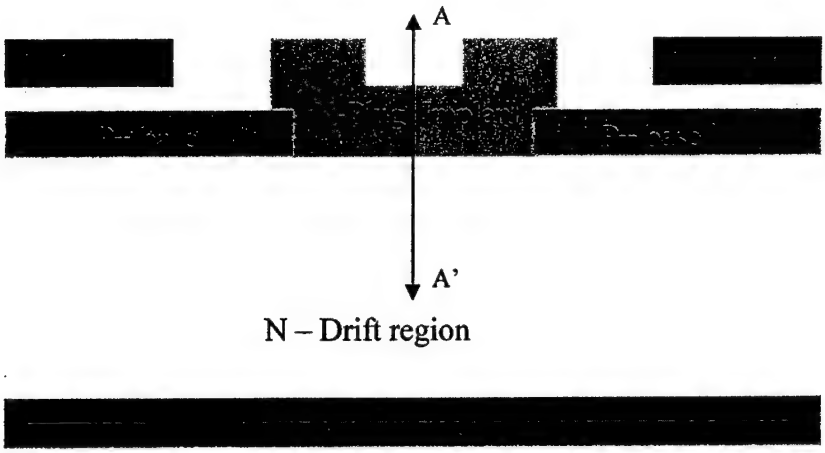
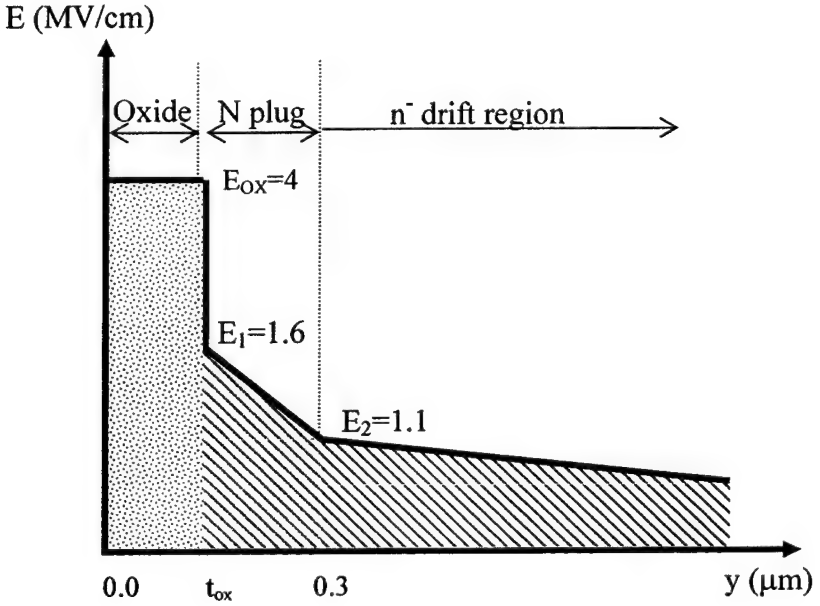


Fig. 3.18. Nitrogen drain plug implantation profile from TRIM simulation.

Figure 3.18 shows the implantation profile of the drain plug implant. The average implanted doping has been chosen to be $2.6 \cdot 10^{17}$ cm^{-3} so that after a 1200°C anneal step, assuming 57% activation, the resulting doping is $1.5 \cdot 10^{17}$ cm^{-3}, and after compensation of the $5 \cdot 10^{16}$ cm^{-3} p channel doping, the final doping of $9.8 \cdot 10^{16} \approx 1 \cdot 10^{17}$ cm^{-3} can be achieved. Figure 3.19a shows the device cross-section after the source and n-type drain plug implantations. The drop in electric field was also calculated, as shown in Fig. 3.19b. For $1 \cdot 10^{17}$ cm^{-3} doping and 0.3 μm epilayer, the drop in field is calculated to be $\Delta E = qN_D t_{epi}/\varepsilon_{SiC}$ = 0.5 MV/cm. With maximum electric field in the oxide at 4 MV/cm, from the dielectric ratio the fields in the semiconductor are E_1=1.6 MV/cm ($1 \cdot 10^{17}$ cm^{-3}) and E_2=1.1 MV/cm ($1 \cdot 10^{15}$ cm^{-3}). Using equation 1.2, the critical electric field calculated for a doping of $1 \cdot 10^{17}$ cm^{-3} is 3.32 MV/cm and for $1 \cdot 10^{15}$ cm^{-3} it is 2 MV/cm. The voltage can be increased by 1.6/1.1= 1.45% before reaching critical electric field in the n^- region.



a) Sample cross-section after the source and n-plug implantation



b) Electric field profile along A-A'

Fig. 3.19. a) Sample cross-section after the phosphorus source and nitrogen drain plug implantation, and b) electric fields in the n-plug region assuming the maximum field in the oxide at 4MV/cm, an n-plug doping of $1 \cdot 10^{17}$ cm^{-3}, and n^- drift region doping of $1 \cdot 10^{15}$ cm^{-3}.

The n-type implants were then simultaneously activated at a temperature of 1200°C for 40 min in argon. Figure 3.20 shows sample photographs after the implantation anneal.

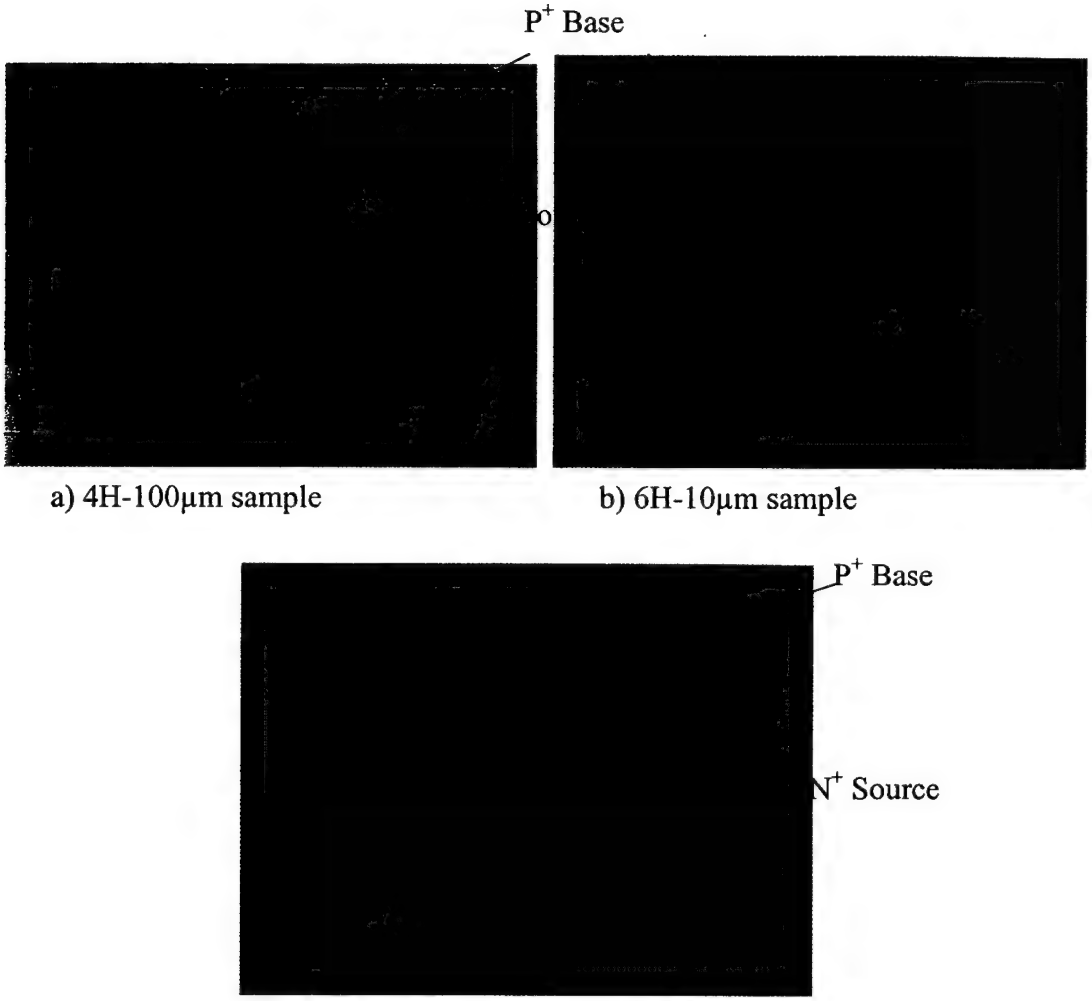
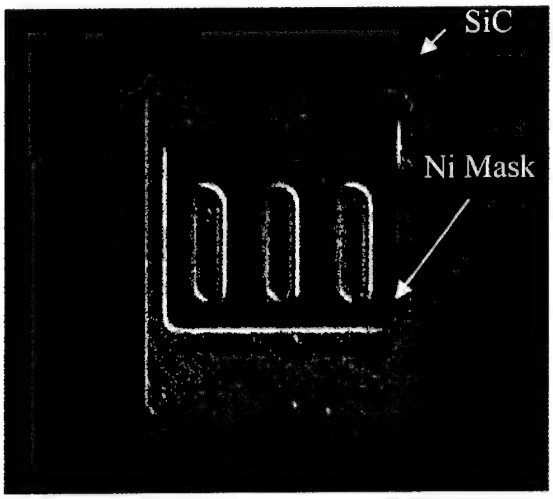
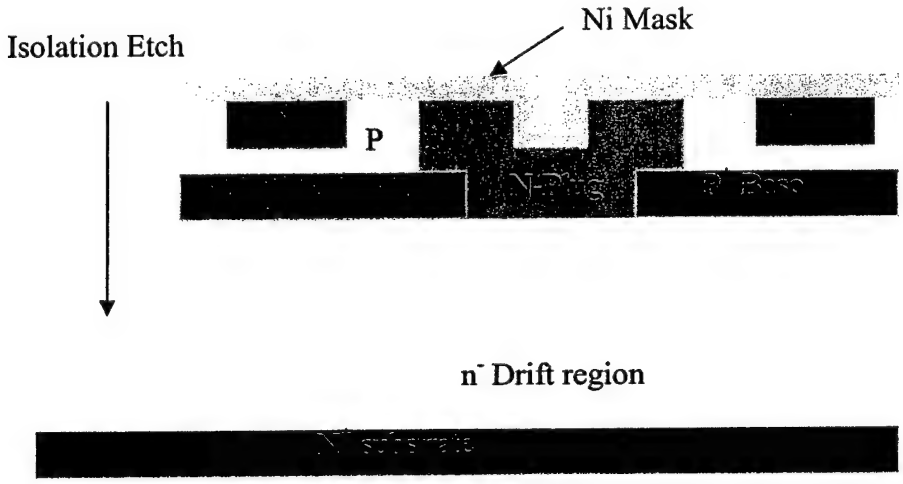


Fig. 3.20. Sample photographs after the phosphorus and nitrogen implantation anneal at 1200^0C for 40 min in an argon ambient.

A sacrificial oxidation of 200^0A was performed before transferring a 1200^0A thick nickel mask by liftoff lithography for the isolation trench. The isolation trench of 1μm was achieved by RIE of SiC. Figure 3.21a) shows a 4H-50 μm sample after the trench etch, and b) shows the sample cross-section at this point.



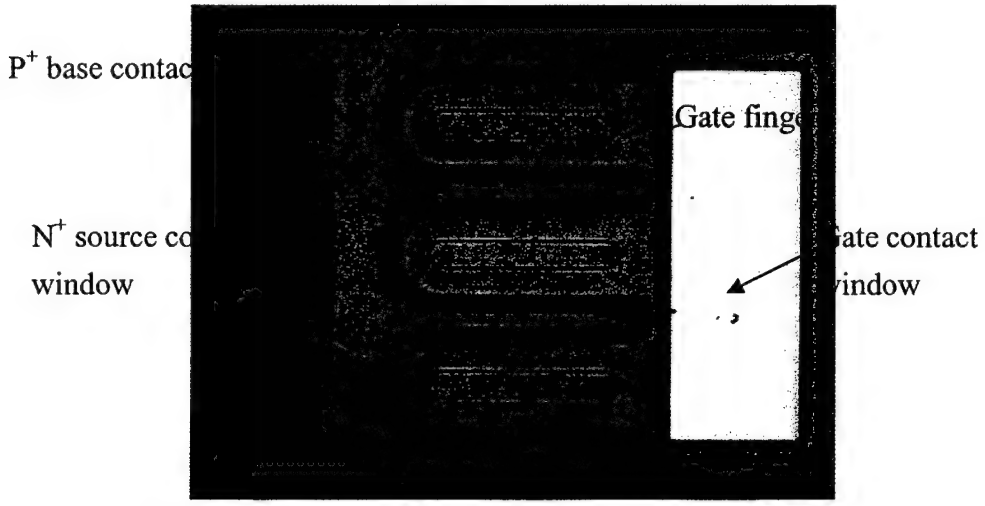
a) 4H-50 μm sample after the trench isolation etch.



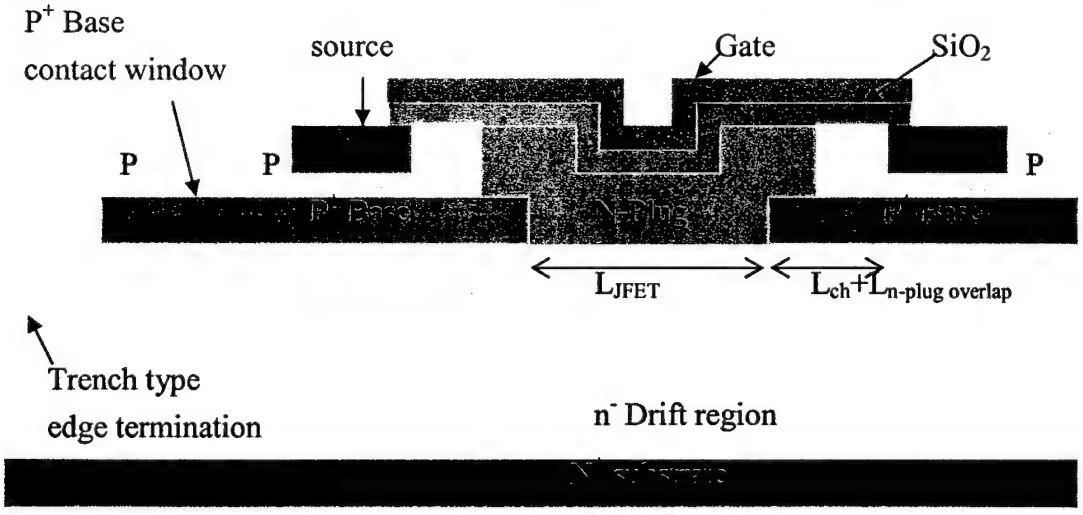
b) Sample cross-section after the trench isolation etch.

Fig. 3.21. Sample photograph after the trench isolation etch and also showing the device cross-section at this point.

The gate oxidation was performed by depositing and oxidizing polysilicon to get the required gate oxide thickness of 1600°A. 0.5 μm of poly was again deposited and heavily doped with phosphorus to form the polysilicon gates. The polysilicon gates were then patterned by RIE. The p^+ base contact and n^+ source contact windows were then opened by etching SiO_2 and polysilicon. 0.3 μm of SiC was etched by RIE to open up the p^+ base contact using Ni as the RIE mask. Figure 3.22a) shows photograph of the final device, and b) shows the cross-section of the final device.



a) Final device with no tapered epi (4H-50 μm sample)

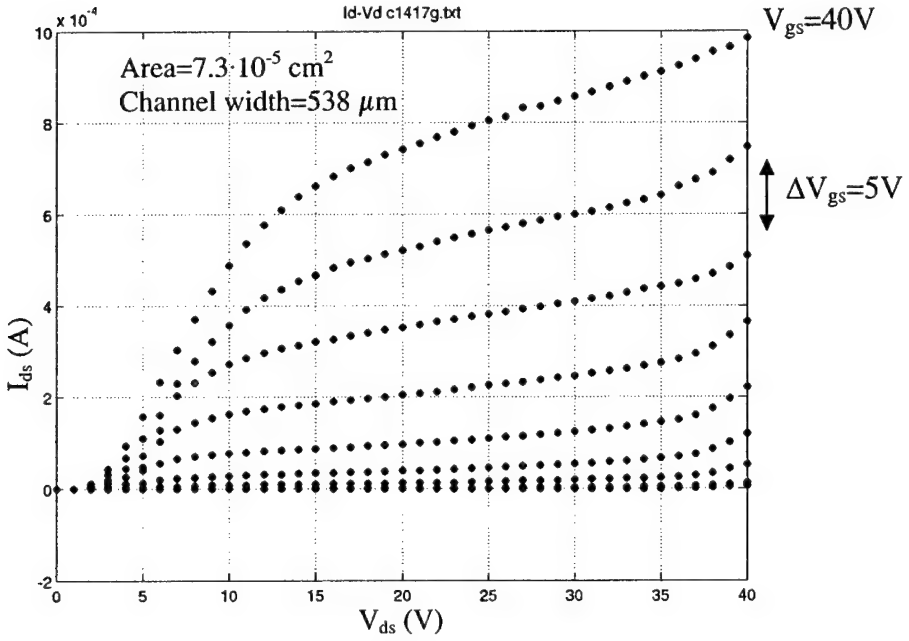


b) Sample cross-section after the trench isolation etch.

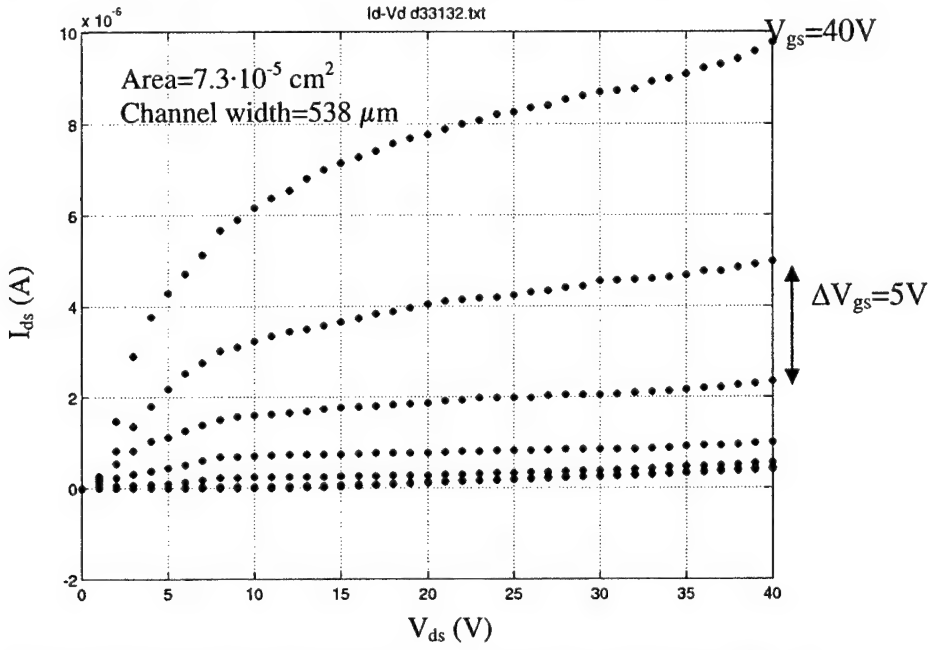
Fig. 3.22. Final device picture with schematic cross-section.

3.5 EpiDMOSFET Results and Discussion

The I-V measurements were performed with an HP4145 parameter analyzer. Measurements were performed before (by direct probing into the SiC) and also after source contact metal deposition and anneal. Figures 3.23a) and b) show the I-V characteristics of epiDMOSFETs in 6H-SiC on a 10 μm epilayer, and in 4H-SiC on a 50 μm epilayer respectively, before source and p-base contact metal deposition and contact anneal. The devices have a channel length of 3 μm, L_{JFET}=12 μm, and plug overlap of 2 μm. The calculated specific on-resistances are 1 Ω-cm^2 and 55.54 Ω-cm^2 respectively. The measurement was performed by grounding the source and base and by varying the drain voltage from 0 to 40 volts for different gate voltages. The I-V curves do not saturate, and even at zero gate voltage there is a current flowing. This is more prominent from the I-V curve (see Fig. 3.24a) for a device in 4H-SiC on a 100 μm epilayer, with L_{ch}=2 μm, $L_{n\text{-plug overlap}}$=2 μm, and L_{JFET}=24 μm, where the device is conducting at 20 volts of drain voltage and zero gate voltage. Monitoring the gate, source, and base currents, we find that this leakage current is actually flowing through the base, which is causing the drain current to increase as shown in Fig. 3.25. Further measurements were performed with nitrogen flow to eliminate any surface leakage phenomenon. The gate leakage was negligible (pA range). The drain current, however, changed with the placement of the probe tip on the p^+ base contact, and increased when the base was left floating (probed outside p^+ contact). With the base grounded, the current flows through the base contact. This is a large reverse-bias leakage current, cause as yet unknown (see Fig. 3.25b). With the base floating, the flow of holes to the base causes the base to float positive, forward biasing the source/base junction, and the increased drain current flows through the source (open base BJT effect).

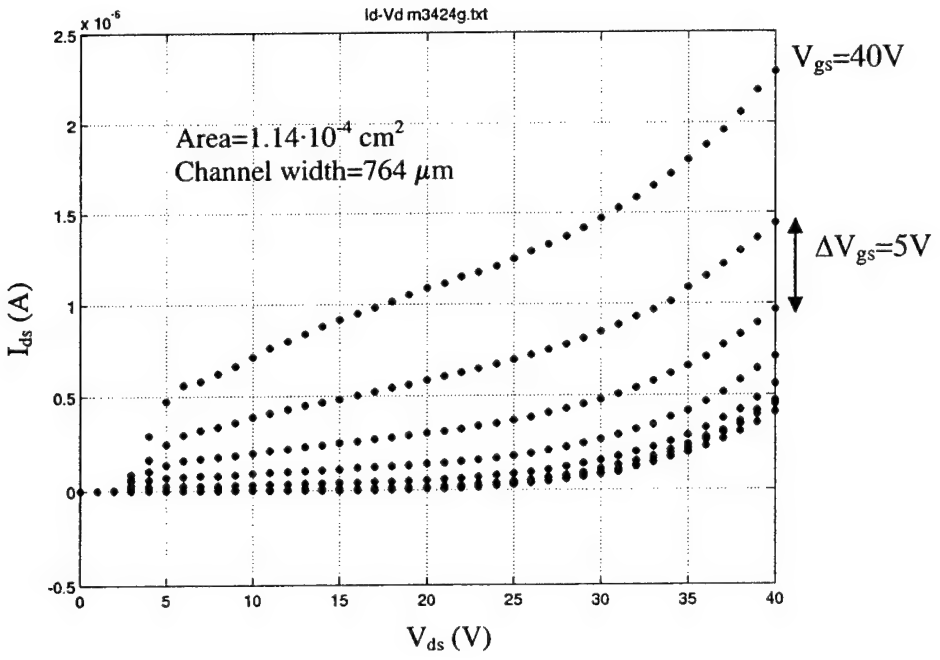


a) I-V characteristics of a device in 6H-SiC on a 10 μm epilayer.

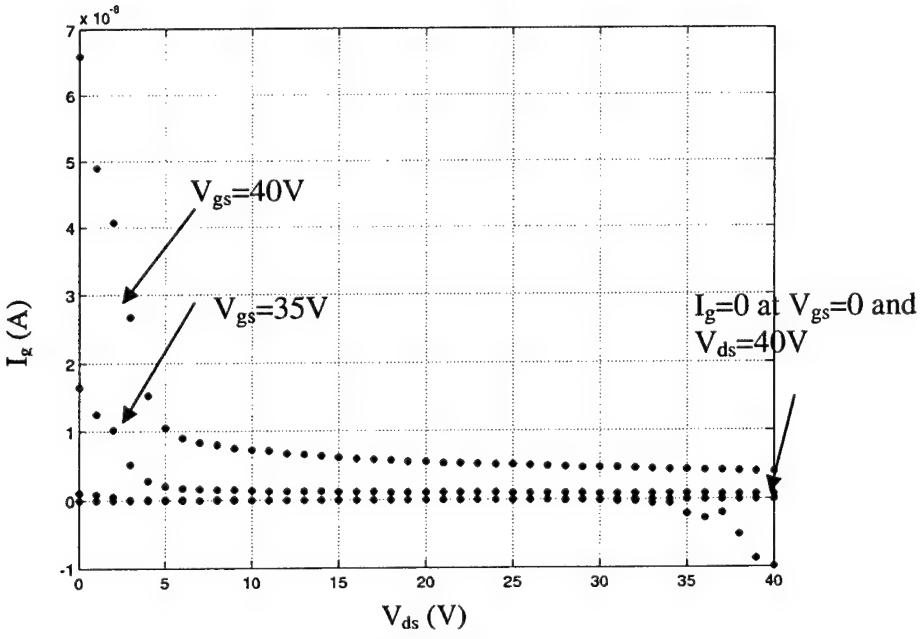


b) I-V characteristics of a device in 4H-SiC on a 50 μm epilayer

Fig. 3.23. I-V measurements of epiDMOSFETs before source and p-base ohmic contact metal deposition.

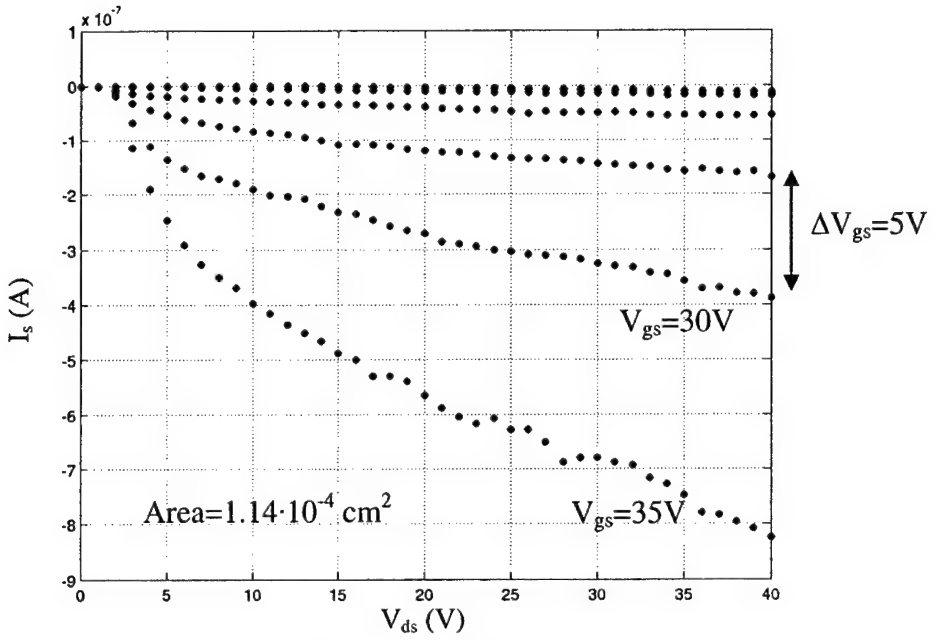


a) Drain current

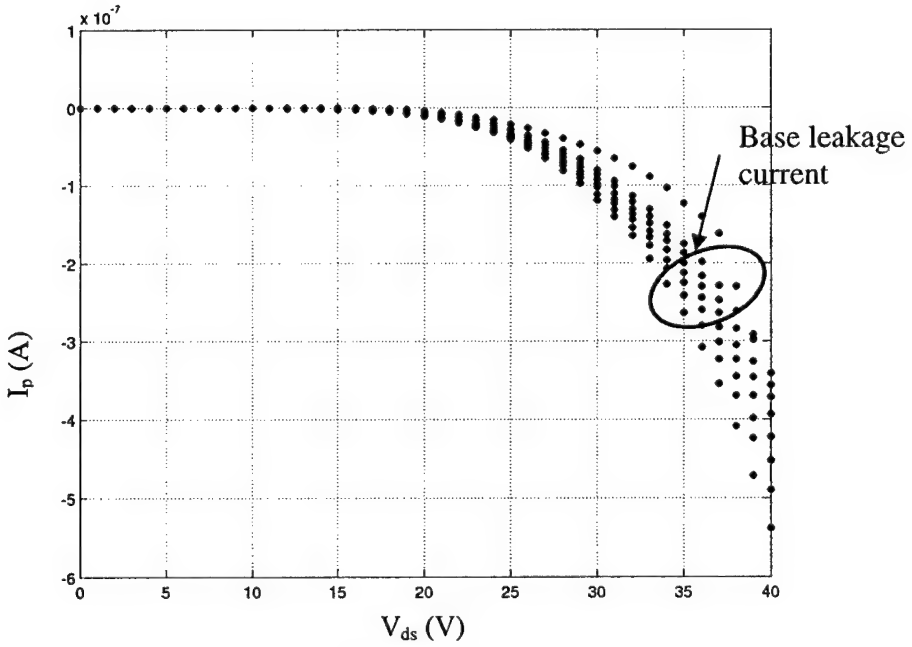


b) Gate current

Fig 3.24. I-V characteristics of a device in 4H-SiC on a 100 μm epilayer before the source and base contact metal depositions. The I_{ds} –V_{ds} curves are non-saturating, even at V_{gs}=0.



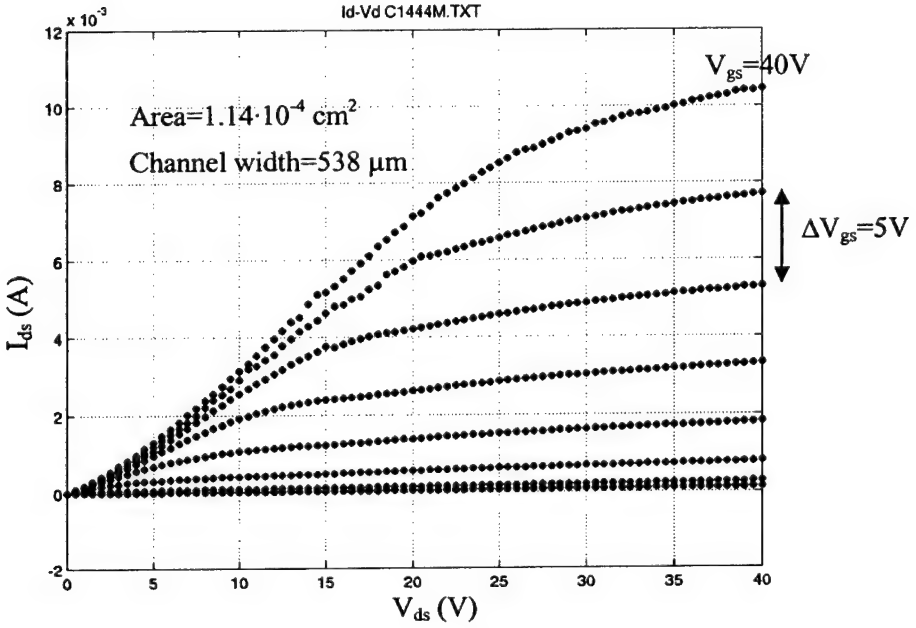
a) Source current



b) Base current

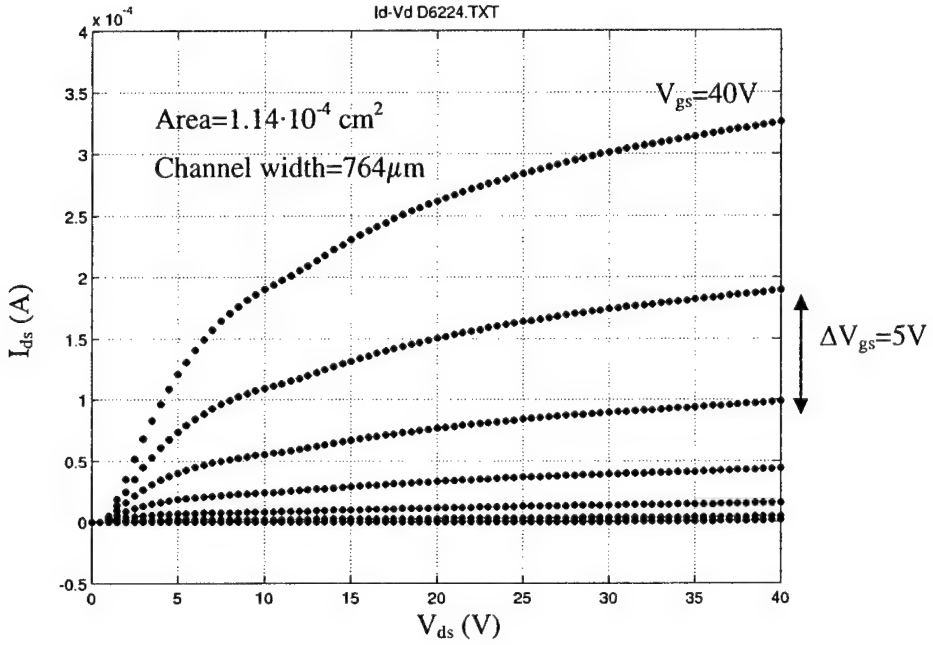
Fig 3.25. Investigating the leakage current phenomenon in MOSFETs. The plots show source and base currents for the device in 4H-SiC on 100 μm epilayer. A large reverse-bias leakage current of 350 nA~540 nA is flowing through the base when V_{gs} is varied from 0 to 35 V and V_{ds} from 0 to 40 V.

The p^+ contact etch of 0.3 μm was very difficult to control, and to prevent any spiking of the Al contact through the thin p^+ base, no metal was deposited on the p^+ regions. 300^0A of Ni was deposited as the source contact by sputtering, and contact annealing of Ni at 900^0C for 2 minutes in vacuum was performed. 300^0A of Ni as top metal was then deposited by e-beam evaporation. Figures 3.26a, b, and c show the I-V curves for a device in 6H-SiC 10 μm epilayer, 4H-SiC 50 μm epilayer, and a 4H-SiC 100 μm epilayer respectively, after the source contact anneal. The specific on-resistances for a device in 6H-SiC on the 10 μm epilayer, 4H-SiC on the 50 μm epilayer, and 4H-SiC on the 100 μm epilayer were calculated to be 317 mΩ-cm^2, 3.2 Ω-cm^2, and 282 Ω-cm^2 respectively.

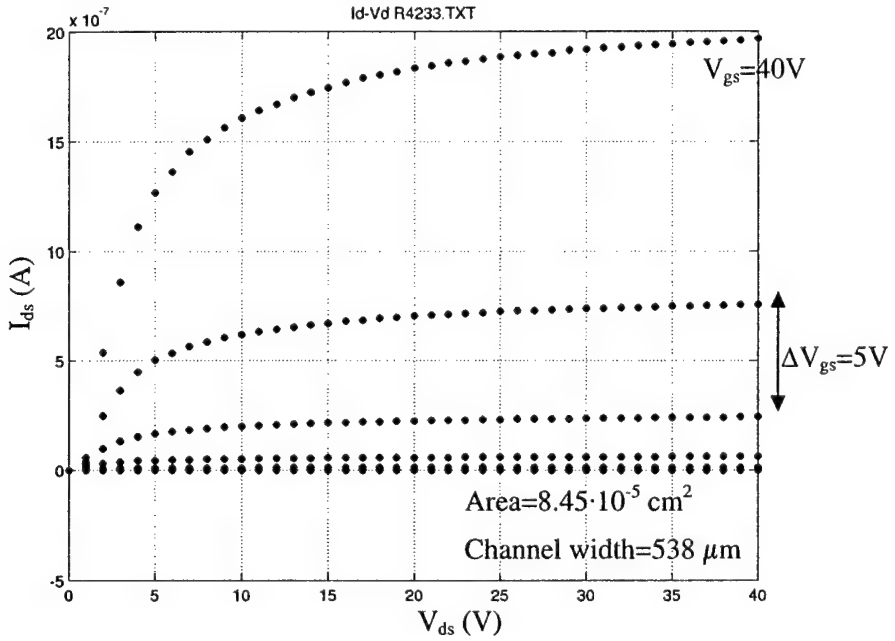


a) I-V characteristics of a device in 6H-SiC on a 10 μm epilayer.

Fig. 3.26. a) I-V measurements of a device in 6H-SiC on a 10 μm epilayer after the source contact metal deposition and contact anneal. The device has a L_{ch}=3 μm, $L_{n\text{-plug overlap}}$=2 μm, and L_{JFET}=24 μm.



b) I-V characteristics of a device in 4H-SiC on a 50 μm epilayer



c) I-V characteristics of a device in 4H-SiC on a 100 μm epilayer

Fig. 3.26. b) I-V measurements of a device in 4H-SiC on a 50 μm epilayer, and c) I-V measurements of a device in 4H-SiC on a 100 μm epilayer after the source contact metal deposition and contact anneal. The device with 50 μm epilayer has a L_{ch}=3 μm, $L_{n\text{-plug overlap}}$=2 μm, and L_{JFET}=24 μm, and the device with 100 μm epilayer has a L_{ch}=4 μm, $L_{n\text{-plug overlap}}$=4 μm, and L_{JFET}=12 μm.

Because of the large base leakage current flowing through these devices, no reverse blocking measurements were performed. The lateral MOSFETs could not be measured, as the p^+ base regions on the FATFETs were accidentally etched due to an error in the mask design. However, inversion channel mobility measured from the vertical MOSFETs were found to be extremely low, and less than 1 cm^2/V-sec

The high specific on-resistance for these devices can be attributed to the following reasons:

1) Uncertainty in the step coverage of the p-type channel region by epitaxial growth over the etched p^+ base regions (due to tapered epi growth problem).

2) Uncertainty in the activation of the n-type drain plug (nitrogen) implants at 1200^0C activation anneal, which, if insufficiently activated, may result in a highly resistive path for the electron flow to the drain.

3) Extremely low inversion channel mobility of less than 1 cm^2/Vsec in the p-type channel region as no gate post-oxidation anneal (NO anneal) was performed.

The extremely high specific on-resistance value was also reported by Dr. Jan Spitz of Purdue University [38], where a similar p-type channel region was epitaxially grown over patterned p^+ base regions in the fabrication of 4H-SiC lateral DMOSFET structures. The mobility value measured from the test MOSFETs (FATFETs) was ~0.001 cm^2/Vsec. The overall anneal temperature for activation of nitrogen implanted source-drain and drain plug region was kept at 1400^0C. While keeping the overall process temperature at 1400^0C, as the p-type inversion channel is replaced by an epitaxilly grown n-type accumulation layer, the channel mobility increased to 9 cm^2/V-sec. The specific on-resistance value was still dominated by the high channel resistance, and reported to be 3.2 Ω-cm^2 on the lateral power FETs.

From the simulation and experimental results, we conclude that the epiDMOS structure is limited by alignment tolerances in the n-plug overlap. In addition to the n-plug region being resistive, the structure was difficult to fabricate as it required a p-type channel epigrowth over an etched p^+ surface. The drain plug region acted like a resistance added to the channel resistance, and a low inversion channel mobility value resulted in a very high specific on-resistance value. From the simulation, the epiAFET structure looked attractive compared to the epiDMOS structure, as it does not require the n-plug implant and therefore does not have the alignment tolerance problem. However, we still

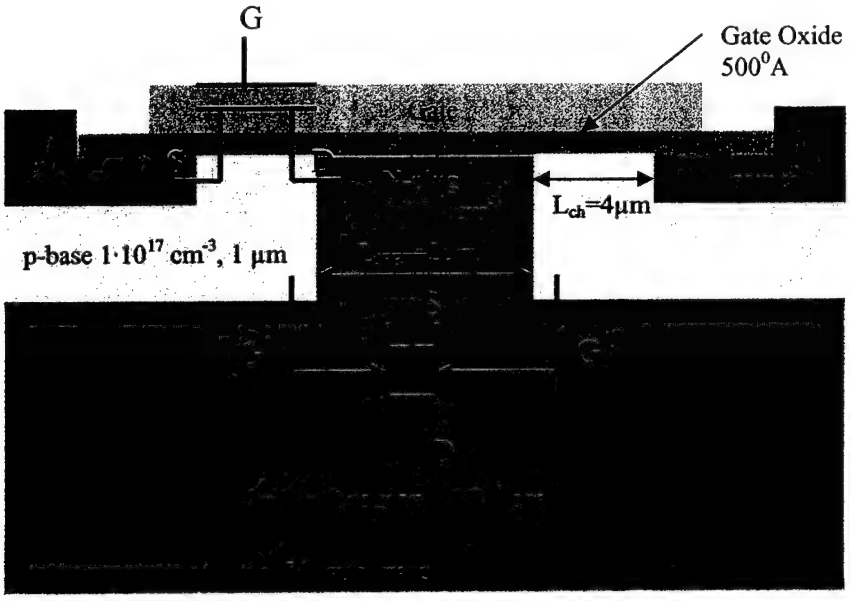
want a normally off device. Although the epigrowth thickness on a whole wafer is within ±25%, the doping can be off by a factor of ±2x, and therefore the threshold voltage in the epiAFET structure is difficult to control. Both the structures require an epigrowth over an etched p^+ surface, and thus we decided not to pursue these structures any further.

4 EPITAXIAL BASE MOSFET: AN ALTERNATIVE DESIGN

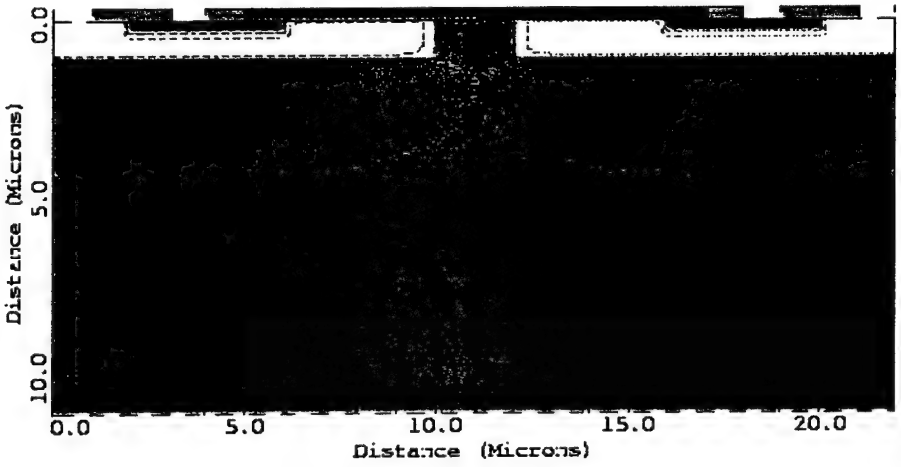
4.1 Device Simulation and Design Study of an Implanted Epitaxial Base DMOS Structure

Conventional DMOSFETs requiring a p-type base implantation suffer from low inversion channel mobility due to surface roughness phenomenon after high temperature (>1700^{0}C) implant activation steps [15]. The epiDMOS structure was then fabricated with a patterened p^+ epitaxial layer, a channel p-type epilayer, and a phosphorus source implant to keep the overall processing temperature ~1200^{0}C [18],[19]. Unfortunately, the step height resulting from patterening the p^+ base layer was difficult to control and the tapered epi problem in the p-type channel region led to discontinuity of the channel. The n-plug region necessary for the epiDMOS structure also acted as a resistive path added to the channel, and low inversion channel mobility resulted in a very high specific on-resistance. In the simulation of the epiAFET structure, the p-type channel epigrowth is replaced by an n-type epigrowth, and does not require the n-type plug implantation. However, both the structures require an epigrowth over the p^+ base region, and are therefore difficult to fabricate. The step in the gate area is also a concern, as sharp corners can lead to early breakdown of the gate. In this chapter, an implanted epitaxial base DMOS structure is studied, where the patterened p^+ base layer is avoided with a single p-type epilyer. Using high energy MeV implantation [39], it is possible to implant species 2-3 μm deep into SiC. This allows us to fabricate DMOS devices with a single p-type epilayer, a deep nitrogen plug implant, and a shallow phosphorus source implant as shown in Fig. 4.1a. The doping and thickness of the p-base layer can be $5\cdot10^{16}$ cm^{-3}, 2μm or $1\cdot10^{17}$ cm^{-3}, 1 μm as long as the total dose is $1\cdot10^{13}$ cm^2, which is necessary to prevent punch through between the source and drain.

At first we decided to use a heavily doped drain plug implant in order to reduce the resistance contribution from the n-plug region The idea was, with the applied drain voltage during off-state, the depletion region in the lightly doped drift layer would extend from both sides, and touch, and this barrier would keep the voltage constant in the heavily doped plug region even with the drain voltage still increasing (see Fig. 4.1b).



a) Schematic cross-section of the implanted epitaxial base DMOS structure.



b) MEDICI simulated implanted epitaxial base DMOS structure.

Fig. 4.1. a) Schematic cross-section of the implanted epitaxial base DMOS structure, and b) MEDICI simulation of the implanted epitaxial base DMOS structure at a drain bias voltage of 8 V. The n-plug doping is $1 \cdot 10^{18}$ cm^{-3}. The dotted line represents the depletion region edges. Note the depletion region extending into the lightly doped n^- drift region with the applied drain bias. The "punch-through" condition is reached at 8 V, while the heavily doped n^+ plug region remains undepleted.

The DMOS structure can be thought of a MOSFET in series with a double gated JFET (see Fig. 4.1a). During the off-state, the MOSFET's gate and source are grounded, the potential of the drain, which is also the source of the JFET (n^+ plug region), increases with the applied drain voltage of the DMOS structure until the depletion region pinches. As the barrier between the n^+ plug and drift region increases, the current through the JFET as well as the MOSFET must decrease. For the subthreshold current of the MOSFET to decrease, the reverse bias voltage in the drain (n^+ plug) must decrease. At steady state, the leakage current flowing through the MOSFET (subthreshold leakage) and the JFET must equal, and the n^+ plug voltage should more or less stay constant at the pinch off voltage. Numerical simulation of the device was performed using a drift region doping and thickness of $1 \cdot 10^{15}$ cm^{-3} and 10 μm respectively on top of a 1 μm thick $8 \cdot 10^{18}$ cm^{-3} doped n^+ substrate. The p-base was 1 μm thick and doped $1 \cdot 10^{17}$ cm^{-3}. A gate oxide thickness of 500°A, a MOSFET channel length of 3 μm, and a JFET length of 2 μm was used in the simulations.

4.1.1 Blocking voltage

Examination of the blocking state was performed by grounding the gate, source, and p-base and by applying a positive voltage to the drain. From simulation, we find that as the drain voltage is increased, the depletion region from the p-base-n^- drift region increases and pinches the region below n^+ plug implant. A 1D electric field slice at the middle of the device revealed that the potential of the undepleted n^+ plug ($1 \cdot 10^{18}$ cm^{-3}) region continued to increase with the increased drain potential beyond pinch off. Figure 4.2 shows the plot of electric field in the oxide versus the applied drain voltage for different doping, thickness, and width (JFET gap) of the n^+ plug region. From the figure we find that the electric field is high for high doping concentration of the plug region and does not depend on the depth or width (L_{JFET}) of the n-plug region.

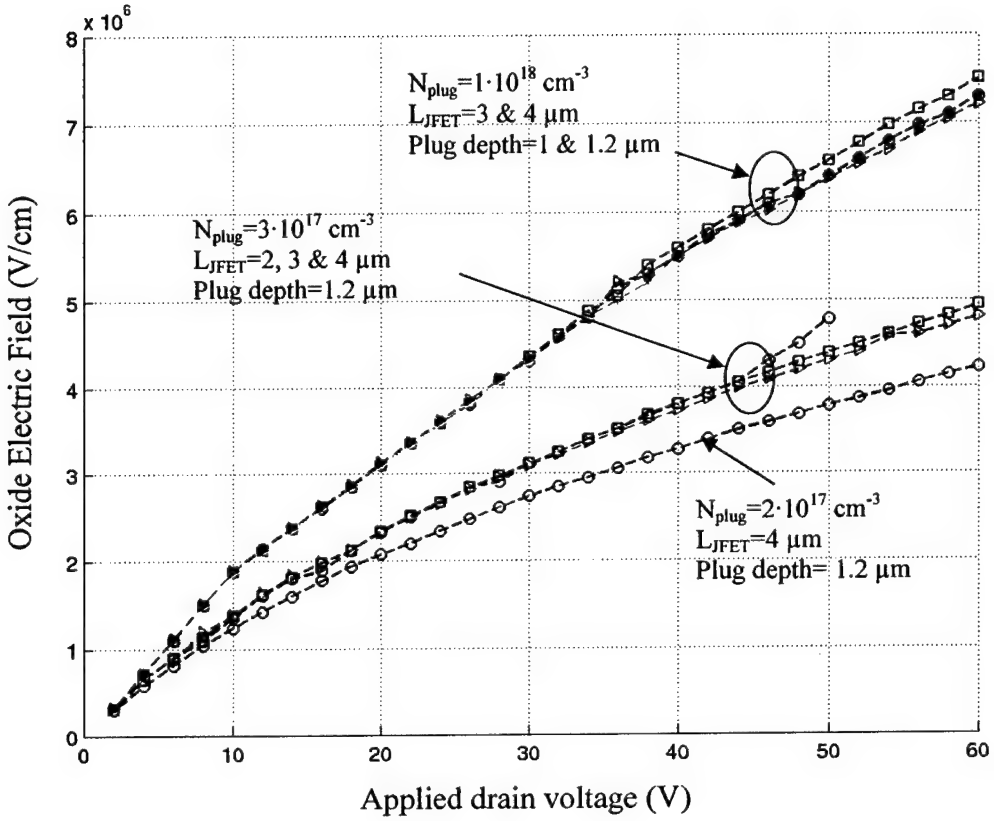
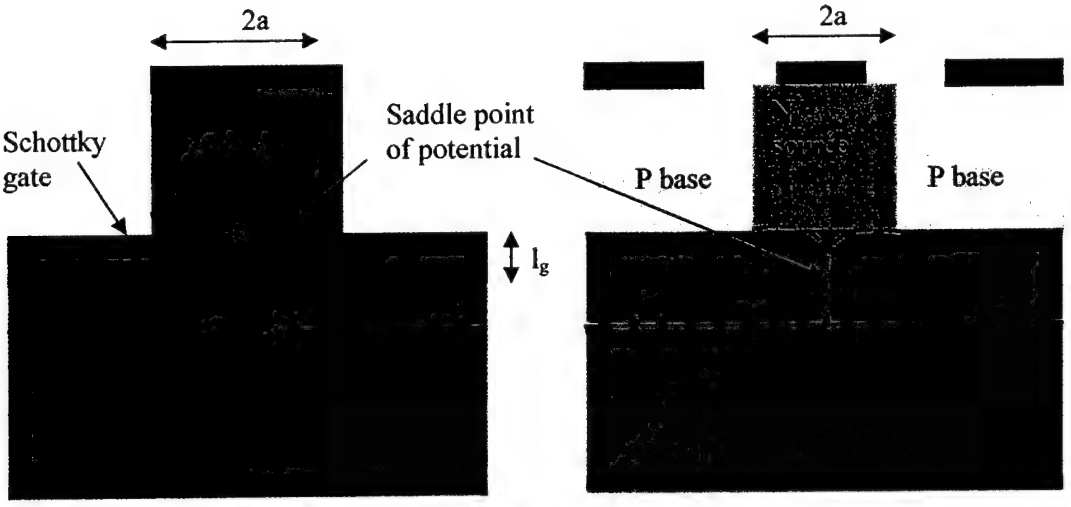
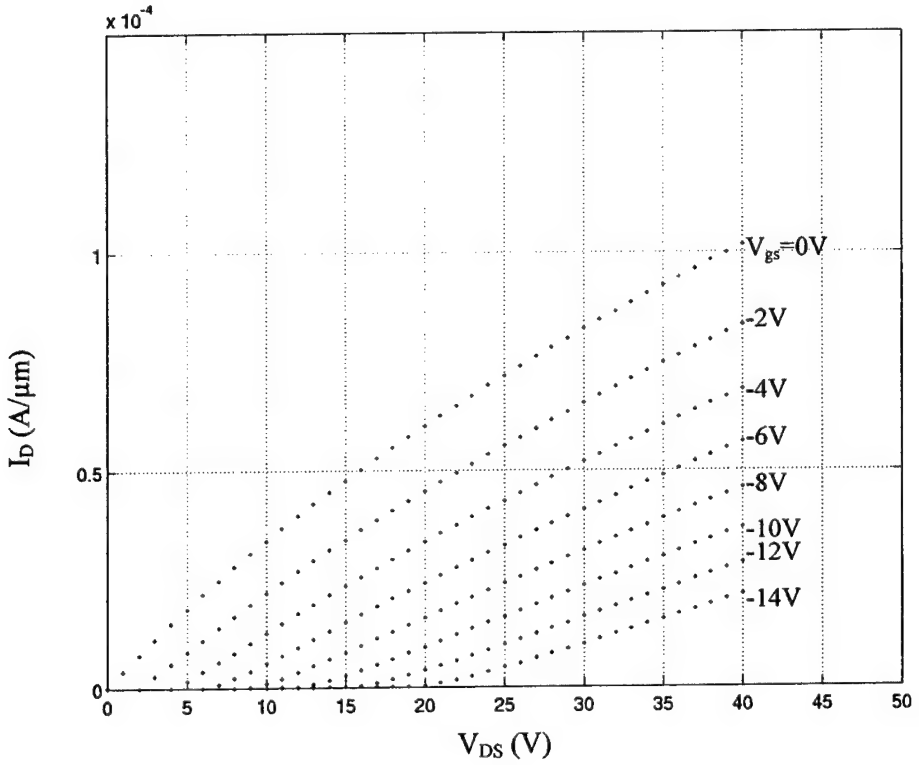


Fig.4.2. Variations in the oxide electric field with the applied drain voltage for different plug doping, width, and depth.

Here, the double gated JFET structure is operating like a static induction transistor (SIT) [40]. In a vertical SIT structure the current is controlled by the Schottky gates, as shown in Figure 4.3a. The n^+ mesa width of '2a' is the channel of the device, and l_g is the gate length (thickness of the Schottky gate). When 'a' is wider than the gate length l_g, then the drain voltage has significant control over the drain current, resulting in non-saturating I-V characteristics. In the simulated double gated JFET structure, the n^+ width is again the channel but the effective gate length l_g (thickness of the p-base) is very short, as it lies entirely over the source (n^+ plug), and the only gating action comes from the fringing fields, making the gate appear to be very short, as shown in Figure 4.3b. For a SIT structure, the I-V curves are non-saturating, as the drain modulates the potential barrier and has significant control over the drain current. When the region between the two gates (p^+ base) is completely depleted, a saddle shaped potential barrier is formed as shown in Fig. 4.3. In order to turn the MOSFET (see Fig. 4.3b) off, we want more coupling from the gate to the saddle point of potential in the channel, and less coupling from the drain to the saddle point. The double gated JFET region showed non-saturating I-V characteristics as shown in Fig. 4.3c.





c) Non-saturating I-V characteristics

Fig. 4.3. SIT (Static Induction Transistor)-like I-V obtained from the double gated JFET region. The p-gate doping was 5e16 cm^{-3} and 2 μm thick. The n^+ source (plug region) doping was 1e18 cm^{-3} and 2 μm thick. A channel length ("2a" dimension) of 2 μm in the JFET region and a channel length of 3 μm in the MOSFET region were used.

In order to prevent premature oxide breakdown, the n-plug doping concentration was therefore changed from $1 \cdot 10^{18}$ cm^{-3} to $5 \cdot 10^{16}$ cm^{-3}. Figure 4.4 shows the schematic cross-section of the simulated implanted epitaxial base DMOS structure. The electric field in the oxide (E_{ox}), the electric fields at the p-base n^- drift region junction (pn#1), and at the p-base n-plug junction (pn#2) were then extracted from the MEDICI simulations. Table 4.1 summarizes all the results extracted from the MEDICI simulations. The gate oxide thickness was 500^0A, the MOSFET channel length (L_{ch}) was 3 μm, and a drift region doping of $7 \cdot 10^{15}$ cm^{-3} and thickness of 10 μm was used.

Table 4.1

N-plug doping (cm^{-3}) and Thickness (μm)	JFET Length (μm)	P-base Doping (cm^{-3}) and Thickness (μm)	Applied Voltage (V)	E_{ox} (MV/cm)	E_{pn}#1 (MV/cm)	E_{pn}#2 (MV/cm)
$5 \cdot 10^{16}$/2.0	4	$5 \cdot 10^{16}$/2.0	1200	5.60	1.42	1.45
			1300	5.70	1.45	1.49
			1400	5.76	1.48	1.51
$5 \cdot 10^{16}$/2.0	2	$5 \cdot 10^{16}$/2.0	1200	4.00	1.32	1.26
			1400	4.10	1.37	1.30
			1500	4.18	1.40	1.33
$E_{critical}$ or $E_{ox,max}$ (MV/cm)				4.00	2.40	3.0

From the simulation we find that even with a low plug doping of $5 \cdot 10^{16}$ cm^{-3}, the field in the oxide with an applied drain bias of 1200 volts is greater than 5 MV/cm (L_{JFET}=4 μm). The oxide electric field can be kept around ~ 4MV/cm by decreasing the JFET length to 2 μm. Figure 4.5 shows the 3D- electric field plot for the simulated structure at an applied voltage of 1500 volts and for a JFET length of 2 μm.

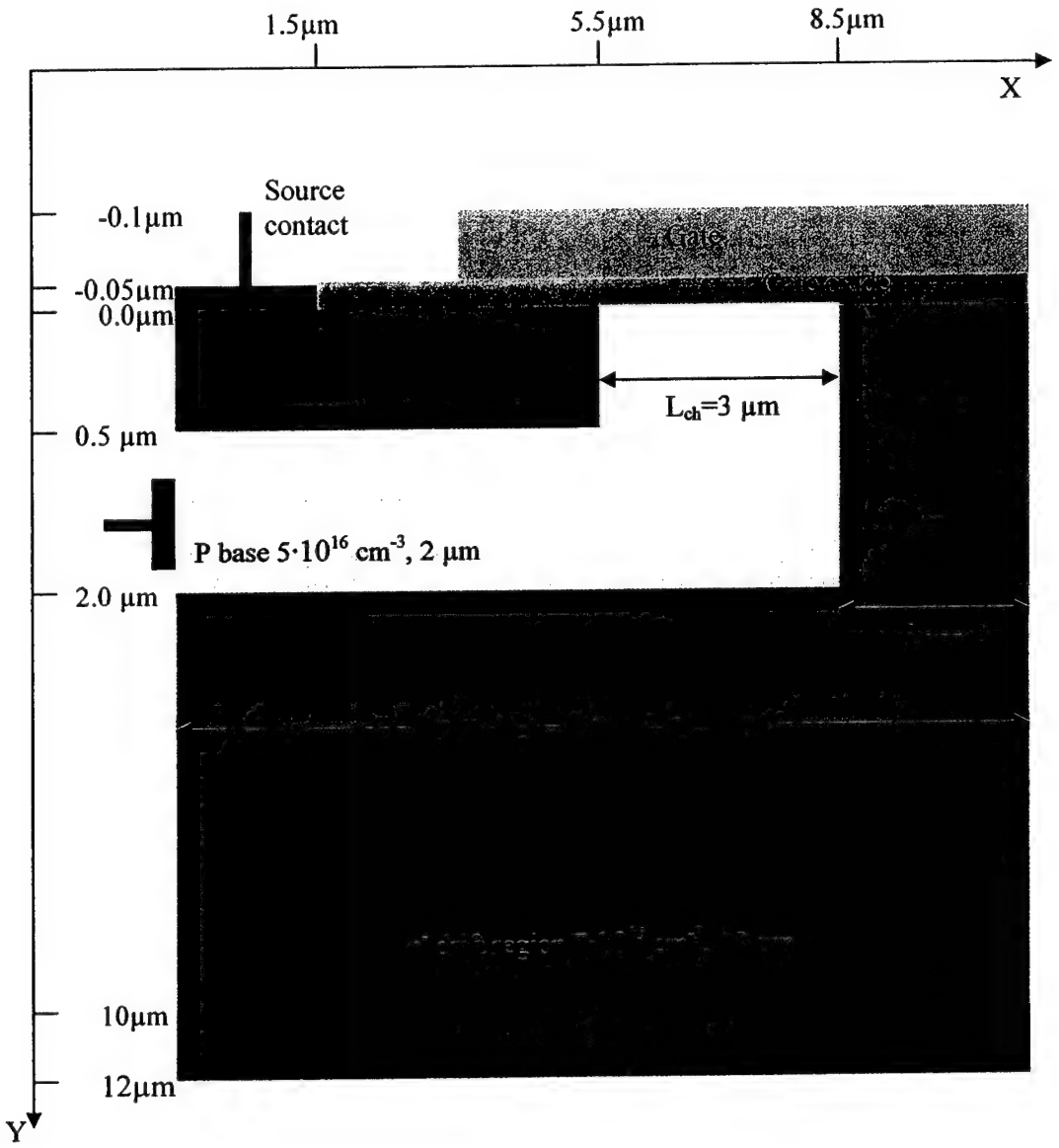


Fig. 4.4. Schematic cross-section of the simulated implanted epitaxial base DMOS structure.

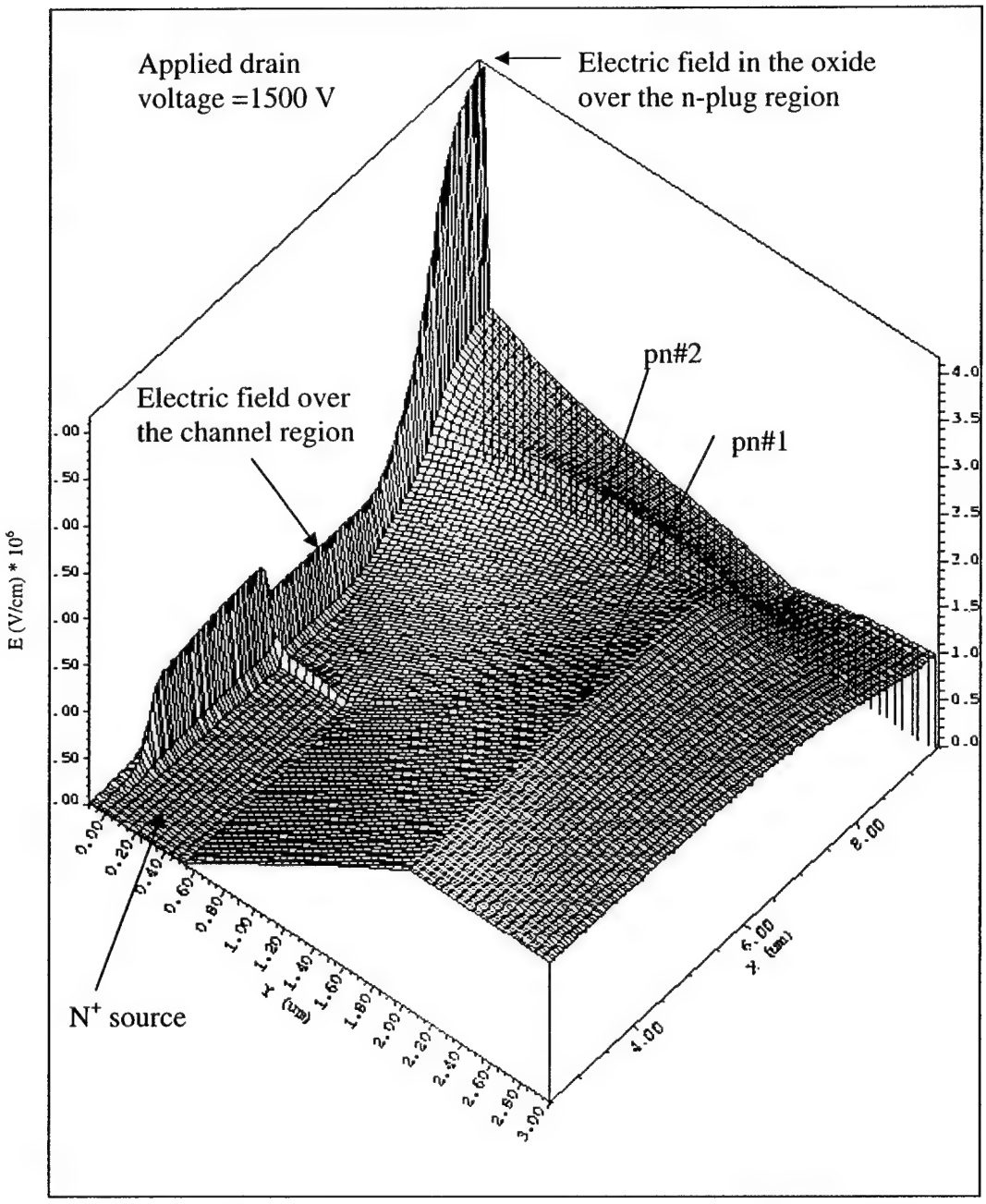


Fig. 4.5. 3D electric field plot for the implanted epitaxial base DMOS structure with a JFET length of 2 μm and a oxide thickness of 500^{0}A.

To avoid premature oxide breakdown at the n-plug region, a thicker oxide over the n-plug region can be used. A second structure with 500^0A over the gate area and 2500^0A over the n-plug region was also simulated. Figure 4.6 shows the schematic cross-section of the "thick-thin" implanted epitaxial base DMOS structure used in the MEDICI simulation. A JFET gap of 4 μm and a MOSFET channel length of 3 μm were used. The drift doping of $7 \cdot 10^{15}$ cm^{-3} and thickness of 10 μm was used. Table 4.2 gives a summary of electric fields for the "thick-thin" epitaxial base DMOS structure.

Table 4.2

N-plug doping (cm^{-3}) and Thickness (μm)	JFET Length (μm)	P-base Doping (cm^{-3}) and Thickness (μm)	Applied Voltage (V)	E_{ox} (MV/cm)	E_{pn}#1 (MV/cm)	E_{pn}#2 (MV/cm)
$5 \cdot 10^{16}$/2.0	4	$5 \cdot 10^{16}$/2.0	1400	2.15	1.42	1.21
			1500	2.22	1.45	1.23
			1600	2.30	1.48	1.25
$1 \cdot 10^{17}$/1.0	4	$1 \cdot 10^{17}$/1.0	1400	2.10	1.36	1.05
			1500	2.15	1.38	1.07
			1600	2.20	1.41	1.10

The field in the oxide can be lowered below 3 MV/cm. A 3D electric field plot for applied drain voltage of 1600V is also shown in Fig. 4.7. A JFET length of 4 μm and n-plug doping of $5 \cdot 10^{16}$ cm^{-3} and thickness of 2 μm was used to simulate the 3D-plot. There is a sharp peak in the electric field at the point of thick-thin oxide transition. The electric field at the p-base- n-plug junction is also high at this point but is still below 3 MV/cm.

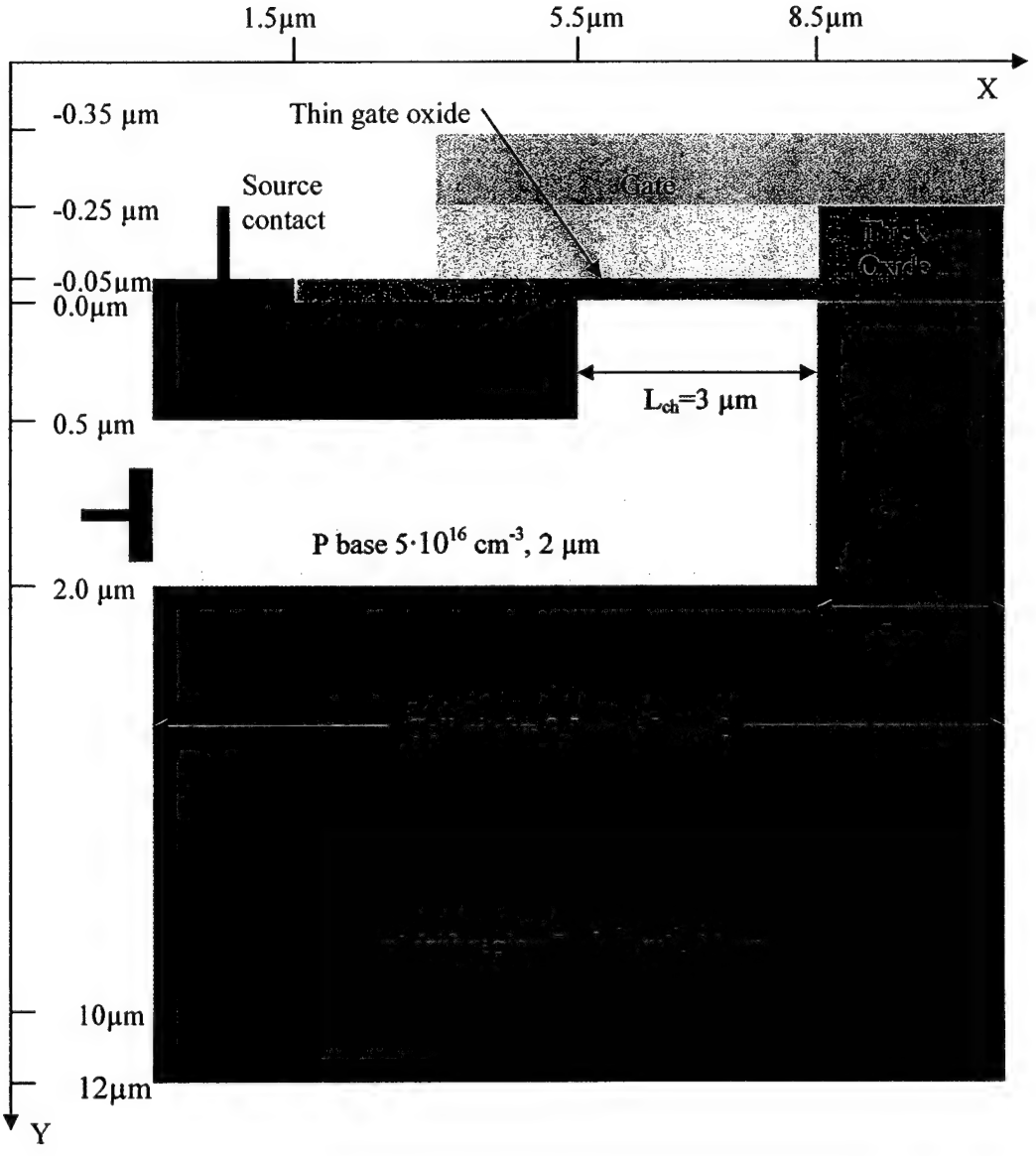


Fig. 4.6. Schematic cross-section of the simulated "thick-thin" implanted epitaxial base DMOS structure.

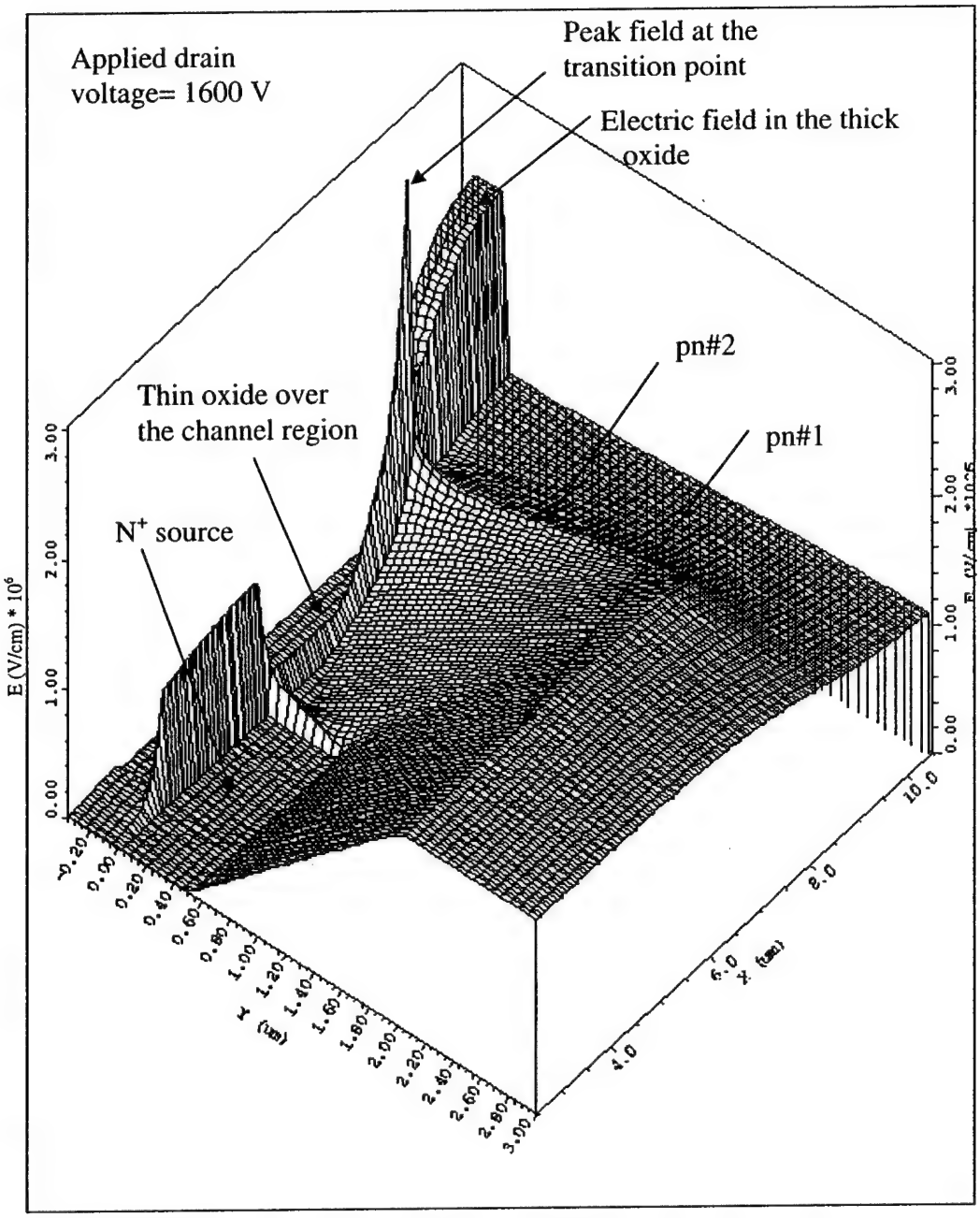


Fig. 4.7. 3D electric field plot for the "thick-thin" implanted epitaxial base DMOS structure.

4.1.2 I-V characteristics

The I-V characteristics were also simulated for a MOSFET channel length of 3 μm, JFET lengths of 2, 3, 4, 5, and 6 μm, and a gate oxide thickness of 500^0A. Figure 4.8 shows the I-V characteristics of the simulated structure for a n-plug doping of $5 \cdot 10^{16}$ cm^{-3}, thickness of 2 μm, and a JFET length of 4 μm. Figure 4.9 shows the corresponding current flow path for a gate voltage of 10V and a drain voltage of 1V. The current flows through the inversion layer formed at the SiC/SiO_2 interface, through the JFET region, and finally spreads uniformly into the drift region. Table 4.3 gives a summary of specific on-resistance calculations for the simulated structure. Inversion channel mobility of 30 $cm^2/Vsec$ was used. The specific on-resistances were then extracted from the linear region of the I-V plots.

Table 4.3

N-plug Doping (cm^{-3}) and Thickness (μm)	P-base Doping (cm^{-3}) and Thickness (μm)	$R_{on\text{-}specific}$ (mΩ-cm^2)					
$5 \cdot 10^{16}$/2.0	$5 \cdot 10^{16}$/2.0	L_{JFET} (μm)	2	3	4	5	6
		Pitch=8.5+L_{JFET}/2 (μm)	9.5	10	10.5	11	11.5
		μ_{ch}=30 $cm^2/Vsec$	15.79	15.39	15.99	16.75	17.51
		$R_{on\text{-}specific}$ (mΩ-cm^2)					
$1 \cdot 10^{17}$/1.0	$1 \cdot 10^{17}$/1.0	L_{JFET} (μm)	2	3	4	5	6
		Pitch=8.5+L_{JFET}/2 (μm)	9.5	10	10.5	11	11.5
		μ_{ch}=30 $cm^2/Vsec$	14.16	14.42	14.77	15.34	15.76

From the simulation we find that the specific on-resistance increases as the JFET gap increases, and is between 15.79-17.51 mΩ-cm^2. The specific on-resistance decreases

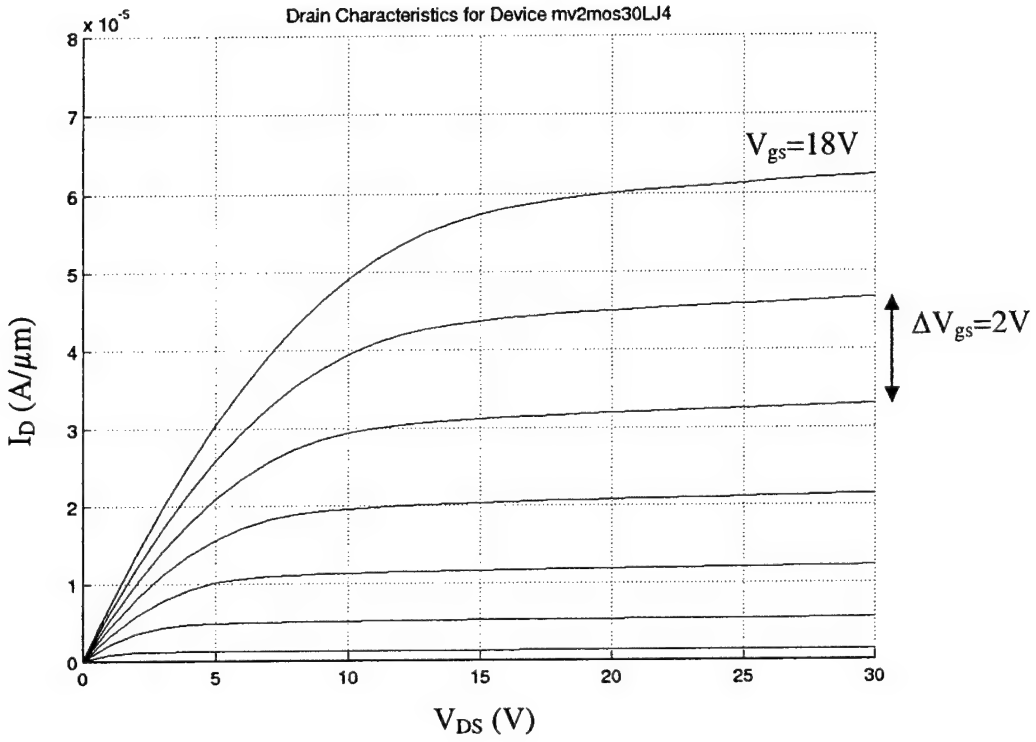


Fig. 4.8. I-V characteristics of the simulated implanted epitxial base DMOS structure with a JFET length of 4 μm, a gate oxide thickness of 500^0A, n-plug doping of $5 \cdot 10^{16}$ cm^{-3}, and thickness of 2 μm.

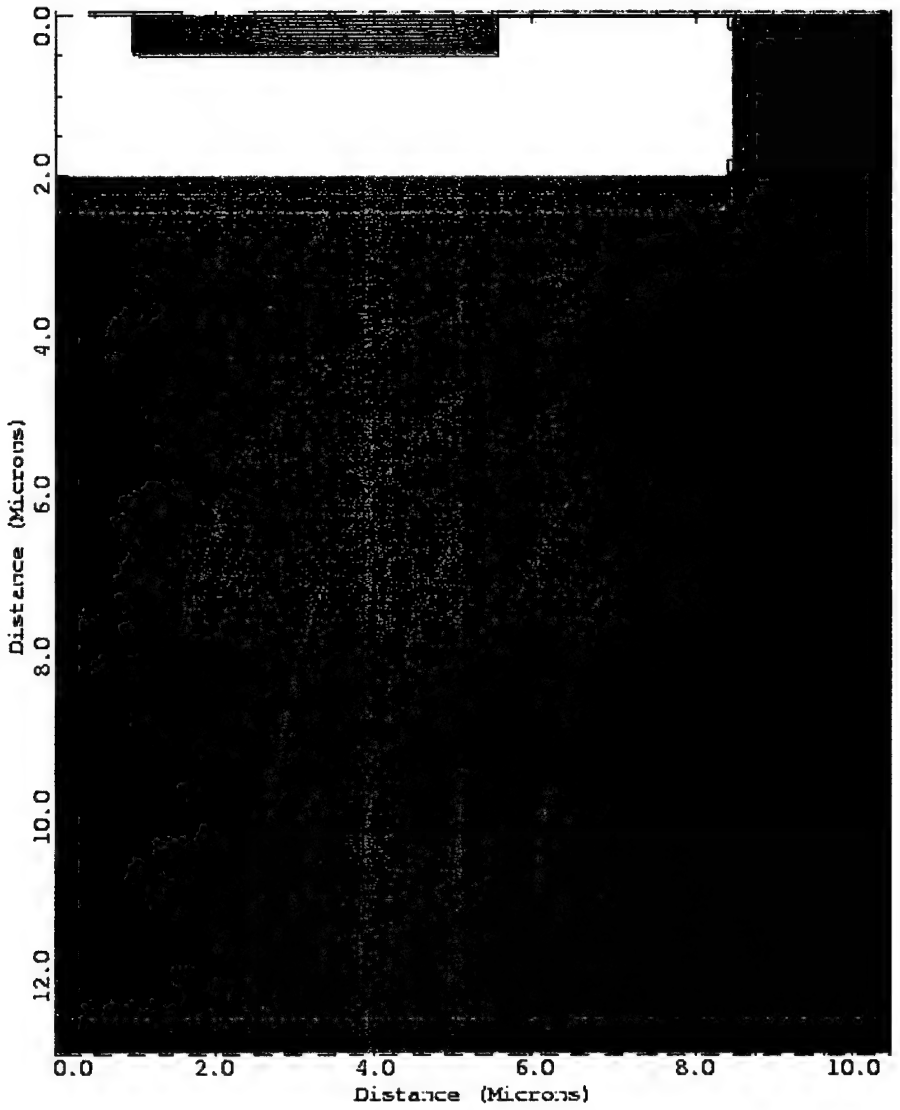


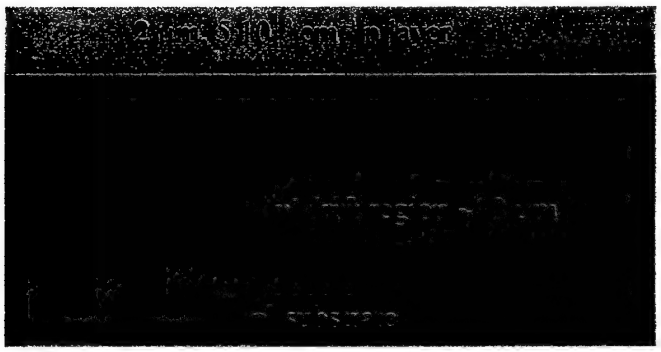
Fig. 4.9. Current flow lines obtained from the implanted epitaxial base DMOS structure at a gate voltage of 10 V and a drain voltage of 1 V.

slightly as the p-base and n-plug doping and thickness are changed to $1 \cdot 10^{17}$ cm^{-3} and 1.0 μm respectively. The $R_{on,sp}$ decreases as the JFET resistance decreases, and again increases as the area of the structure increases. For a plug doping of $1 \cdot 10^{17}$ cm^{-3} we need to used a thicker oxide over the n-plug region to prevent oxide breakdown. The sharp electric field at the thin-thick oxide transition point is also a concern as the n-plug doping is increased. Thus, with this design we don't see any significant improvement on the specific on-resistance, but the blocking voltage capability can be increased to 1600 volts provided a thicker oxide is used over the n-plug region.

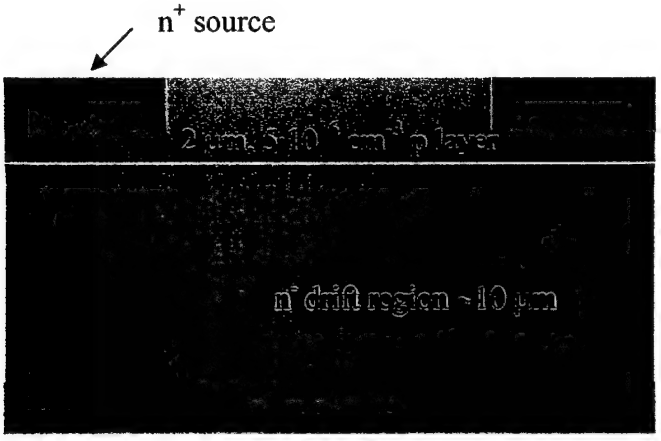
4.2 Process Flow of "Thick-Thin" Implanted Epitaxial Base DMOS Structure

The suggested process flow for the fabrication of 'thick-thin' DMOS structure is described in Fig. 4.10. [41]. The special features are stated below:

1) In this design the conventional retrograde p-type implant needed for DMOS structure is replaced by an epitaxialy grown p-layer with appropriate doping and thickness.
2) Nitrogen or phosphorous can be used as source implants.
3) An n-type plug implant is required to establish the connection between the channel and the drain. A thick Si_3N_4 layer can be sputtered and later patterned to serve as the high energy (MeV) n-type drain plug implant mask. From TRIM simulation we find that nitrogen can be implanted ~2.5 μm deep into SiC with 4 MeV implantation energy. The thickness of the Si_3N_4 layer to block the 4 MeV energy implant needs to be approximately 2.5 μm thick.
4) Activation of the implants can be kept below 1200^0C.
5) A 2000°A thick oxide is then evaporated on top of the Si_3N_4 mask. With H_3PO_4 etchant, the etch rate is medium for Si_3N_4 and very slow (requires etching temperature 'hot') for SiO_2 [42], and therefore, the Si_3N_4 layer can be removed leaving the thick oxide over the n-plug region. However, this requires a large amount of lateral etching of Si_3N_4 from underneath the SiO_2 layer and may become difficult to realize. A 500°A thermal oxidation then can be performed to form the gate oxide over the channel region.

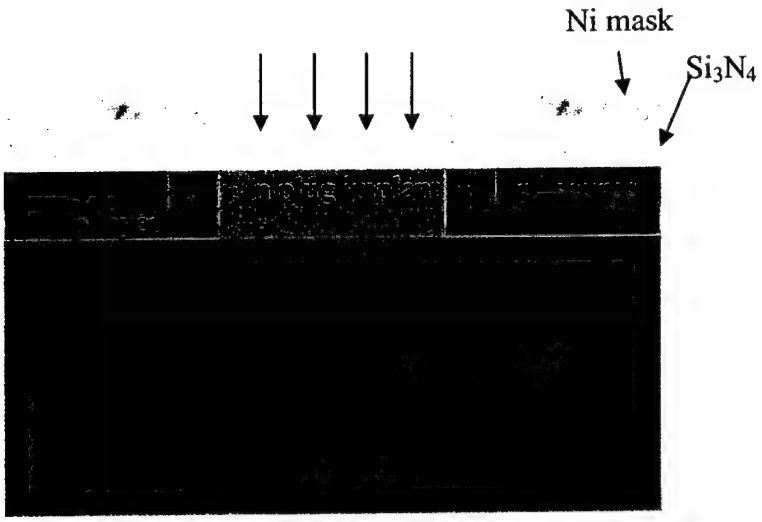


a) Starting wafer structure

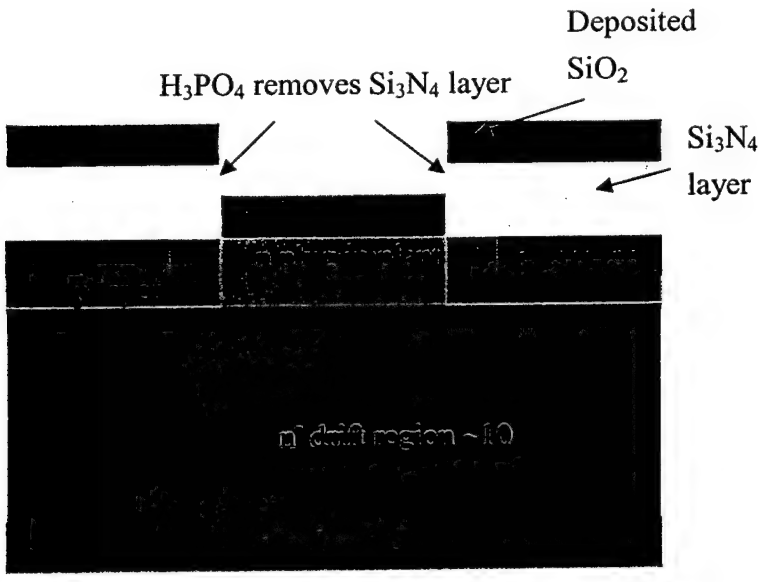


b) Implant n^+ sources

Fig. 4.10. Process flow of "thick-thin" implanted epitaxial base DMOSFET.

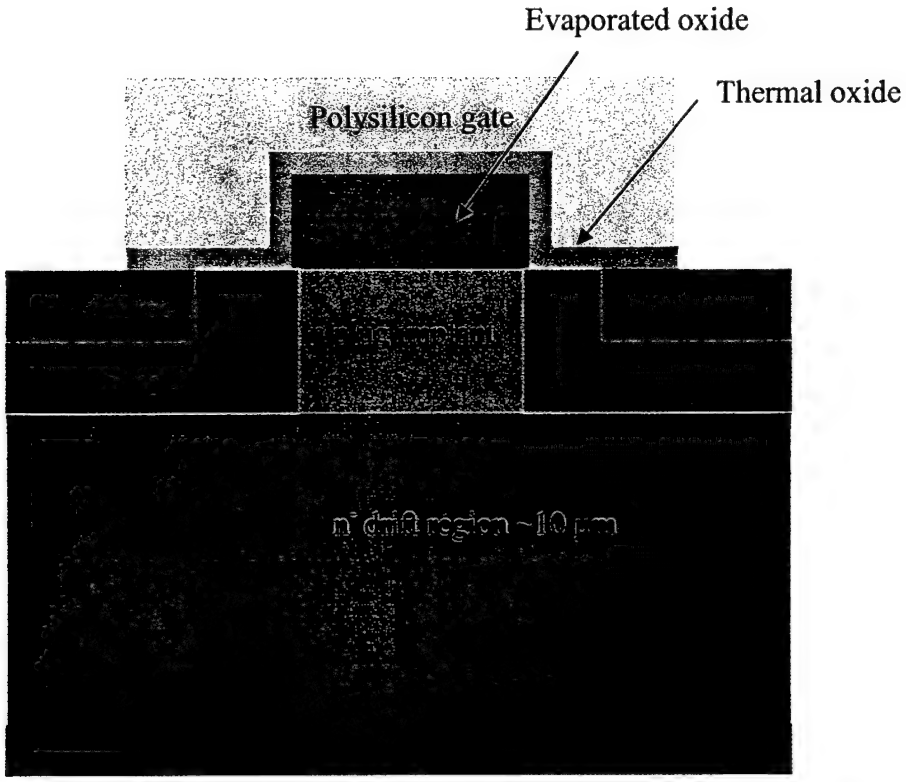


c) Sputter Si_3N_4 and pattern for the n-drain plug implant



d) Deposit thick oxide

Fig. 4.10. Process flow of "thick-thin" implanted epitaxial base DMOSFET (continued)



e) Thermal oxidation and polysilicon gate deposition

Fig. 4.10. Process flow of "thick-thin" implanted epitaxial base DMOS structure.

From the simulation and design study we conclude that, with the implanted epitaxial base DMOS structure, a factor of 1.1 times improvement on the blocking voltage can be obtained compared to the epiDMOS and epiAFET structures, provided a thicker oxide over the n-plug region and a thinner oxide over the gate region are accomplished. The epitaxial base DMOS design is still limited by a high cell pitch and a large channel length, since we have to allow lengths for realistic fabrication processes,

and thus, no improvement on the on-state can be obtained. The n-type implantation necessary for making connection from the channel to the substrate may also act as a resistive path added to the channel length, and if not activated properly, can lead to a high specific on-resistance value. Therefore, we decided not to fabricate this device experimentally.

5. A SHORT CHANNEL 4H-SIC DMOSFET STRUCTURE

5.1 Motivation for a Short Channel 4H-SiC DMOS Structure

The 4H-SiC polytype is the polytype of choice for power MOSFET applications due to its high critical electric field (E_{crit}, MV/cm), higher bulk mobility, and less mobility anisotropy compared to the 6H polytype. However, the inversion channel mobility (μ_{ch}, $cm^2/Vsec$) is very poor, and consequently the specific on-resistance ($R_{on-specific}$, $m\Omega\text{-}cm^2$) is completely dominated by the resistance from the channel region. The channel length of a DMOSFET (L_{ch}, μm) is the distance between the edges of the ion implanted n^+ source and the p-base region. In order to allow for alignment tolerance during the photolithographic process, the channel length is limited to about 2 to 3 μm. The specific on-resistance is the product of the total on-resistance and the active area (Area=cell pitch, S x width, W) of the device. By reducing the channel length, the specific on-resistance of the device can be reduced, as the resistance contribution from a long channel with low inversion layer mobility is reduced, and also as the cell pitch is reduced. This section describes a design study performed on the DMOS structure by EXCEL calculations and MEDICI simulations. The specific on-resistance and the blocking voltage are modeled for a DMOS structure with 0.5 μm and 3 μm channel lengths.

5.2 Modeling the Specific On-Resistance of the DMOS Structure

During the on-state, as a positive voltage is applied to the gate, an inversion channel is formed, and with a positive voltage applied to the drain, current flows through the channel, through the JFET region, and finally through the drift region into the n^+ substrate. The current flow through the device is then determined by the total on-state resistance $R_{on,sp}$, which is the sum of $R_{channel,sp}$, $R_{source,sp}$, $R_{JFET,sp}$ and $R_{Drift,sp}$. To model the specific on-resistance of the DMOS structure, the analytical model of power silicon MOSFETs proposed by Sun and Plummer [43] will be used.

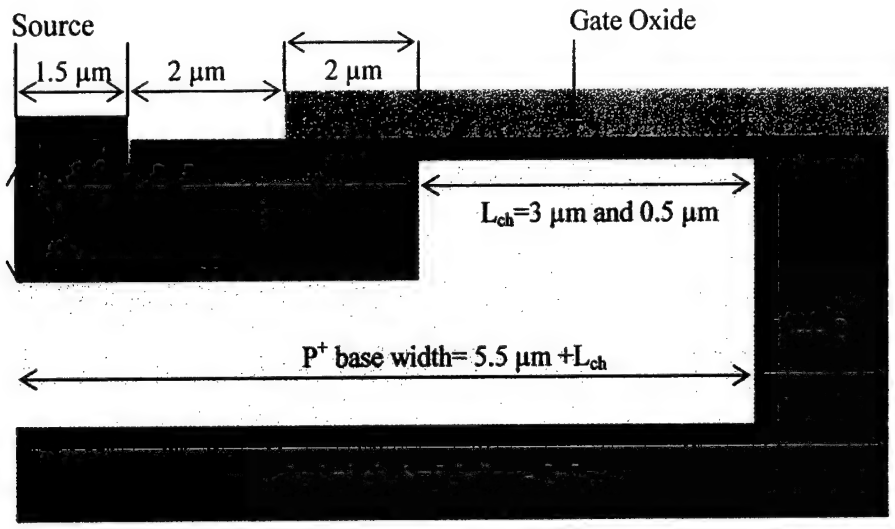


Fig. 5.1. Calculation of the channel and source specific on-resistance.

I. Channel Resistance

The structure used for EXCEL calculations of the channel and source resistances is shown in Fig. 5.1. The channel specific on-resistance is:

$$R_{channel,sp} = \frac{L_{ch} S}{\mu_{ch} C_{ox} (V_G - V_T)} \tag{5.1}$$

where L_{ch} is the channel length, S is the cell pitch, μ_{ch} is the electron mobility in the inversion channel, C_{ox} is the gate capacitance per unit area, and V_T is the threshold voltage. The term C_{ox} (V_G-V_T) equals the inversion charge (Q_{inv} C/cm^2) in the inversion layer. The total charge per unit area in the semiconductor Q_s is the sum of the inversion charge Q_{inv}, the bulk charge Q_{bulk}, and any charge at the oxide/semiconductor interface due to fixed oxide charges Q_F or charges in interface traps Q_{it}. From Gauss's law

$Q_s=\varepsilon_s E_s=\varepsilon_{ox}E_{ox}$. If we neglect the bulk charge in the semiconductor and introduce a factor γ, which represents the fraction of charge induced in the inversion layer and not into the interface traps, then equation (5.1) can be written as:

$$R_{channel,sp}=\frac{L_{ch}S}{\mu_{ch}\varepsilon_{ox}\gamma(E_{ox,V_G}-E_{ox,V_T})} \tag{5.2}$$

where $E_{ox,VG}$ is the oxide field at the applied gate voltage V_G, and $E_{ox,VT}$ is the oxide field at threshold. For simplicity, we have assumed γ=1, and $Q_{it}=Q_F=0$. For EXCEL calculations, the maximum field in the oxide is limited to $E_{ox,VG}=E_{ox,max}$= 4 MV/cm and the inversion channel mobility value of 30 cm^2/Vsec was used.

II. Source Resistance

The source resistance can be expressed as:

$$R_{source,sp}=\left(\rho_s L_{SN+}+\frac{\rho_c}{L_T}\right)S \tag{5.3}$$

where ρ_s is the sheet resistance ($\Omega/\square$) of the N^+ source region, L_{SN+} is the length of the source region, ρ_c is the specific contact resistance (Ω-cm^2), and L_T is the transfer length. The transfer length $L_T=\sqrt{(\rho_c/\rho_s)}$ is defined as the length where the voltage drop due to current flowing from semiconductor to metal or metal to semiconductor drops to 1/e of its maximum value. Typical values of resistivities are ρ=0.015 Ω-cm for a doping of $1\cdot10^{19}$ cm^{-3}, ρ=0.024 Ω-cm for a doping of $5\cdot10^{18}$ cm^{-3}, and ρ_c=1e-4 Ω-cm^2. Here for an n^+ source implant depth of 0.3 μm, ρ_s=500 $\Omega/\square$ ($1\cdot10^{19}$ cm^{-3}) and ρ_s=800 $\Omega/\square$ ($5\cdot10^{18}$ cm^{-3}) and the source specific on-resistance becomes $R_{source,sp}$=0.87S Ω-cm^2 and $R_{source,sp}$=0.987S Ω-cm^2 respectively.

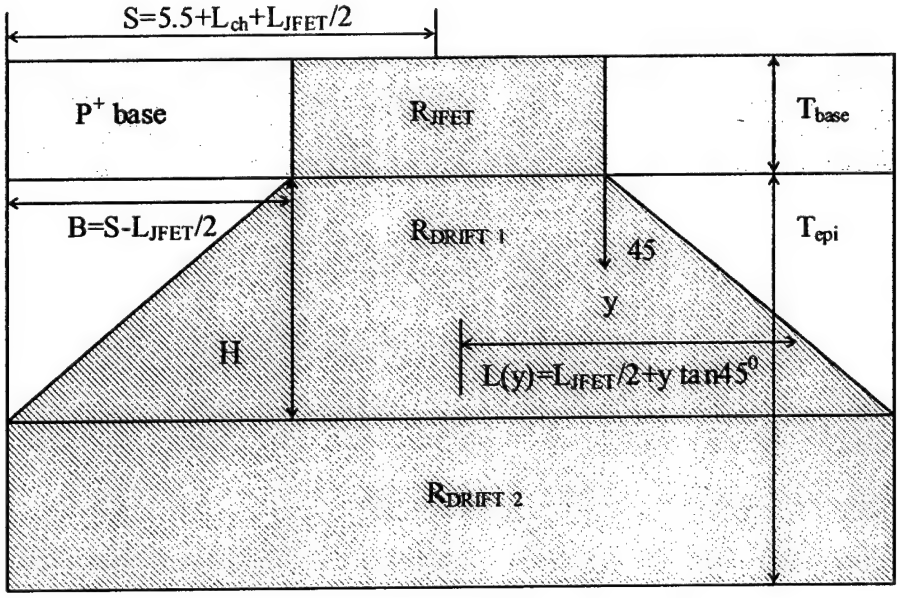


Fig. 5.2. DMOS structure used to calculate the JFET and drift region resistances.

III. JFET Resistance

A junction field effect transistor (JFET) exists between the adjacent p-base regions as shown in Fig. 5.2. To calculate the JFET resistance, the current flow is assumed to originate from the SiO_2/SiC surface and flow uniformly downward until it reaches a distance T_{base} from the surface. The JFET specific on-resistance is then given by

$$R_{JFET,sp} = \frac{\rho T_{base} S}{L_{JFET}/2} \tag{5.4}$$

where ρ is the resistivity of the n^- drift region, T_{base} is the thickness of the implanted p^+ base region, and L_{JFET} is the distance between the adjacent p-base regions. In EXCEL calculations, the depletion extension (X_{depl}) from the p^+ base region into n^- JFET region was also taken into account, and assumed a 1 volt reverse voltage across the pn junction between the p^+ base and the n-type JFET region due to the voltage drop across the MOS channel in the conducting state. The depletion region largely extends into the lightly

doped n^- region, and this pinches the current flow and increases the JFET resistance. The $R_{JFET,sp}$ is then estimated by

$$R_{JFET,sp} = \frac{\rho(T_{base} + X_{depl})S}{(L_{JFET}/2 - X_{depl})} \tag{5.5}$$

IV. Drift Resistance

The drift region resistance is the sum of the spreading resistance $R_{DRIFT\,1}$ and $R_{DRIFT\,2}$. To calculate the $R_{DRIFT\,1}$ we have assumed that current spreads out uniformly from the JFET region into the drift region over the trapezoidal volume with a spreading angle of 45^0 (the electron mobility parallel and perpendicular to the c-axis differ by only about 10% in 4H-SiC). If we assume y is positive downward below the JFET region, then the current density is given by

$$J(y) = \frac{I}{WL(y)} = \frac{1}{\rho}\frac{dV}{dy} \tag{5.6}$$

where W is the width of the device perpendicular to the plane of the drawing in Fig. 5.2 and ρ is the resistivity of the drift region. By substituting the trapezoidal length, $L(y) = L_{JFET}/2 + y\tan 45^0 = L_{JFET}/2 + y$ in equation 5.6, the $R_{DRIFT1,sp}$ is then calculated by performing a resistance integral along the drift length up to y=H, where $H=B=(S-L_{JFET}/2)$ and $H<T_{epi}$. The $R_{DRIFT\,1\,,sp}$ is then estimated by

$$R_{DRIFT1} = \frac{\rho}{W}\int_0^H \frac{dy}{(L_{JFET}/2 + y)} \tag{5.7}$$

$$R_{DRIFT1,sp} = \rho S \ln\left(1 + \frac{H}{L_{JFET}/2}\right) \tag{5.8}$$

Now if the depletion from the heavily doped p-base into the lightly doped drift region is taken into account, the $R_{DRIFT\,1,sp}$ is estimated by equation 5.9.

$$R_{DRIFT1,sp} = \rho S \ln\left[1 + \frac{(S - L_{JFET}/2 + X_{depl})}{(L_{JFET}/2 - X_{depl})}\right] \tag{5.9}$$

where $H=B+2X_{depl}$. The $R_{DRIFT\ 2,sp}$ part is calculated assuming uniform current flow and is given by

$$R_{DRIFT2,sp} = \rho(T_{epi} - H) \tag{5.10}$$

When the depletion into the drift region is taken into account then the expression is given as:

$$R_{DRIFT2,sp} = \rho(T_{epi} - B - 2X_{depl}) \tag{5.11}$$

5.3 Modeling the Blocking Voltage

In the blocking mode of operation, the gate, source, and p-base are grounded and a positive voltage is applied to the drain. The breakdown voltage is determined by the onset of avalanche due to the impact ionization process, which occurs when the electric field across the supporting p^+n^- junction becomes large. At high electric fields, the thermally generated carriers are accelerated to high velocities. At some critical value of electric field (E_{crit}), the carriers can gain sufficient kinetic energy so that when they collide with an atom in the lattice, the energy released can create an electron-hole pair. All three carriers are again accelerated by the electric field, gain kinetic energy, and upon collision can create additional electron-hole pairs. The avalanche condition is reached when the ionization integral reaches unity, as follows [3]:

$$\int_0^W \alpha_p \exp\left[-\int_0^y (\alpha_p - \alpha_n)dy\right]dy = 1 \tag{5.12}$$

where α_p and α_p are hole and electron impact ionization coefficients (cm^{-1}). The ionization rates vary exponentially with the inverse of electric field, and are given by equation 4.9 (a) and (b). In modeling the breakdown voltage of the DMOS structure, the ionization integral excludes the depletion regions into the heavily doped p^+ -base and n^+

substrate, as most of the depletion region extends into the lightly doped n^- drift region. To calculate the breakdown voltage numerically by solving the ionization integral, first we calculate the electric field inside the semiconductor as a function of position by solving Poisson's equation (4.1). The electric field in terms of the maximum field at the p^+n^- junction and depletion width are expressed as follows:

$$E(y) = |E_{\max}| - \frac{qN_D}{\varepsilon_{SiC}} y \tag{5.13}$$

$$|E_{\max}| = \frac{qN_D W}{\varepsilon_{SiC}} \tag{5.14}$$

$$W = \sqrt{\frac{2\varepsilon_{SiC}(V_{bi} - V_{applied})}{qN_D}} \tag{5.15}$$

These equations are valid for a non-punch through device where $W < t_{epi}$. The ionization integral is then calculated using ionization coefficients from equation (4.9), and the $V_{applied} = -V_{Drain}$ is increased until the ionization integral equals unity. The breakdown voltage is then the area under the triangular electric field profile as shown in Fig. 5.3 and the critical electric field $E_{crit}=E_{max}$ is the maximum electric field at which the impact ionization condition is met. The breakdown voltage for a non-punch through structure is then expressed as follows:

$$V_{BR} = \frac{E_{crit} W}{2} = \frac{\varepsilon_{SiC} E_{crit}^2}{2qN_D} \tag{5.16}$$

In a punch-through design, the depletion region width $W > t_{epi}$. In these devices, as the applied voltage is increased, the depletion region extends and punches through to the n^+ substrate. The maximum electric field at punch-through is E_{PT}, and the punch-through voltage V_{PT} is the area under the triangular electric field profile as shown in Fig. 5.3, expressed as follows:

$$V_{PT} = \frac{E_{PT} t_{epi}}{2} = \frac{qN_D t_{epi}^2}{2\varepsilon_{SiC}} \tag{5.17}$$

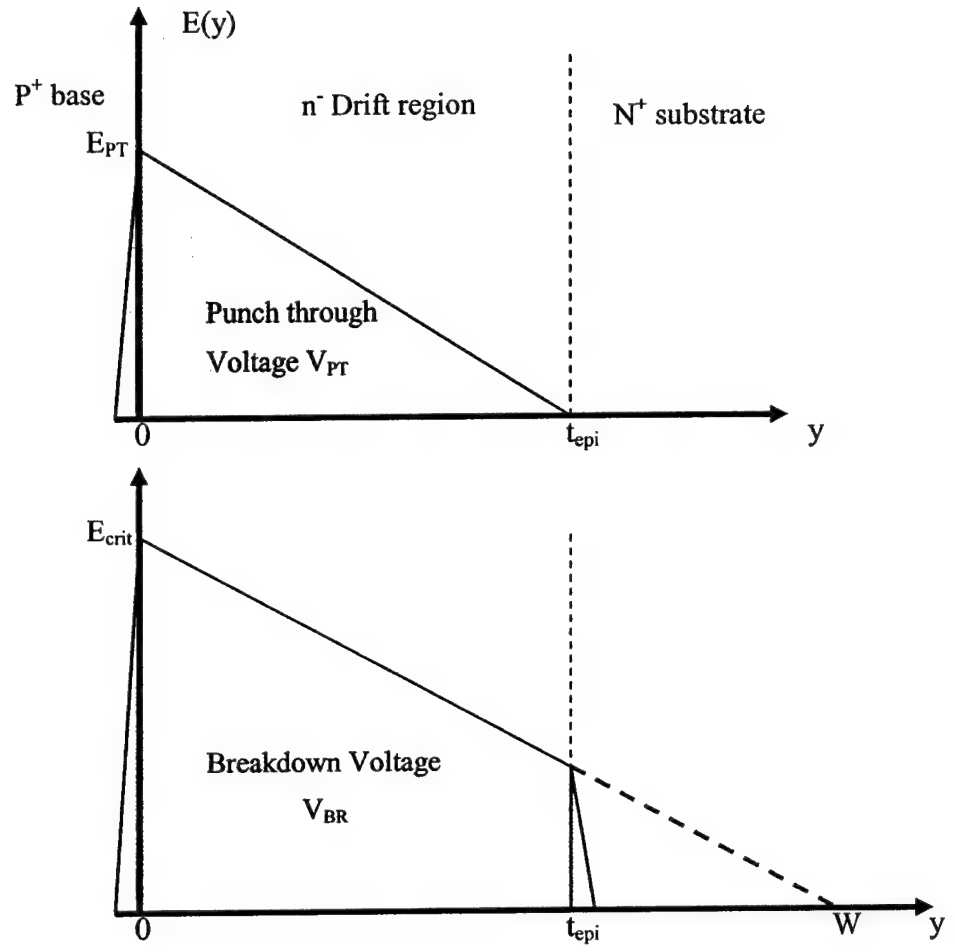


Fig. 5.3. Electric field profile at punch-through (top) and at breakdown (bottom) in a "punch-through" structure.

The breakdown voltage of a punch-through structure is the area under the trapezoidal electric field profile as shown in Fig. 5.3. The breakdown voltage in terms of the critical electric field and punch-through voltage can be expressed as:

$$V_{BR} = E_{crit} t_{epi} - V_{PT} \tag{5.18}$$

The equation is also valid for the non-punch through structure, since by substituting t_{epi}=W and V_{PT}=V_{BR} we arrive at equation (5.16). The plot of breakdown voltage, which was obtained by solving the ionization integral numerically as a function of doping and epilayer thickness, is shown in Fig. 5.4. As we go from high to low doping, the breakdown voltage increases, but the specific on-resistance also increases with the decrease in doping. The strongly punched-through structures do not show any doping dependence of the blocking voltage.

For the design of power MOSFETs, there is a design trade off between the minimum specific on-resistance and the maximum blocking voltage. In high voltage devices, the drift layer is lightly doped and thicker and therefore suffers from high specific on-resistances. From Figure 5.4 we find that the optimum design for the non-punch through structure requires the epilayer thickness to be equal to the depletion width at breakdown condition. In this way we get the minimum specific on-resistance for the designed blocking voltage. In this section in order to estimate the specific on-resistances, EXCEL calculations were performed on 1kV to 8kV designed blocking voltages with appropriate dopings and thicknesses. The optimum drift layer doping and thickness value as a function of the designed blocking voltages were obtained from [44]. The relations are summarized in Table 5.1 for n-type 4H-SiC drift regions.

Table 5.1

Optimum Drift Layer Thickness (μm)	$2.62 \times 10^{-3} (V_{BR})^{1.12}$
Optimum Drift Layer Doping (cm^{-3})	$1.10 \times 10^{20} (V_{BR})^{-1.27}$

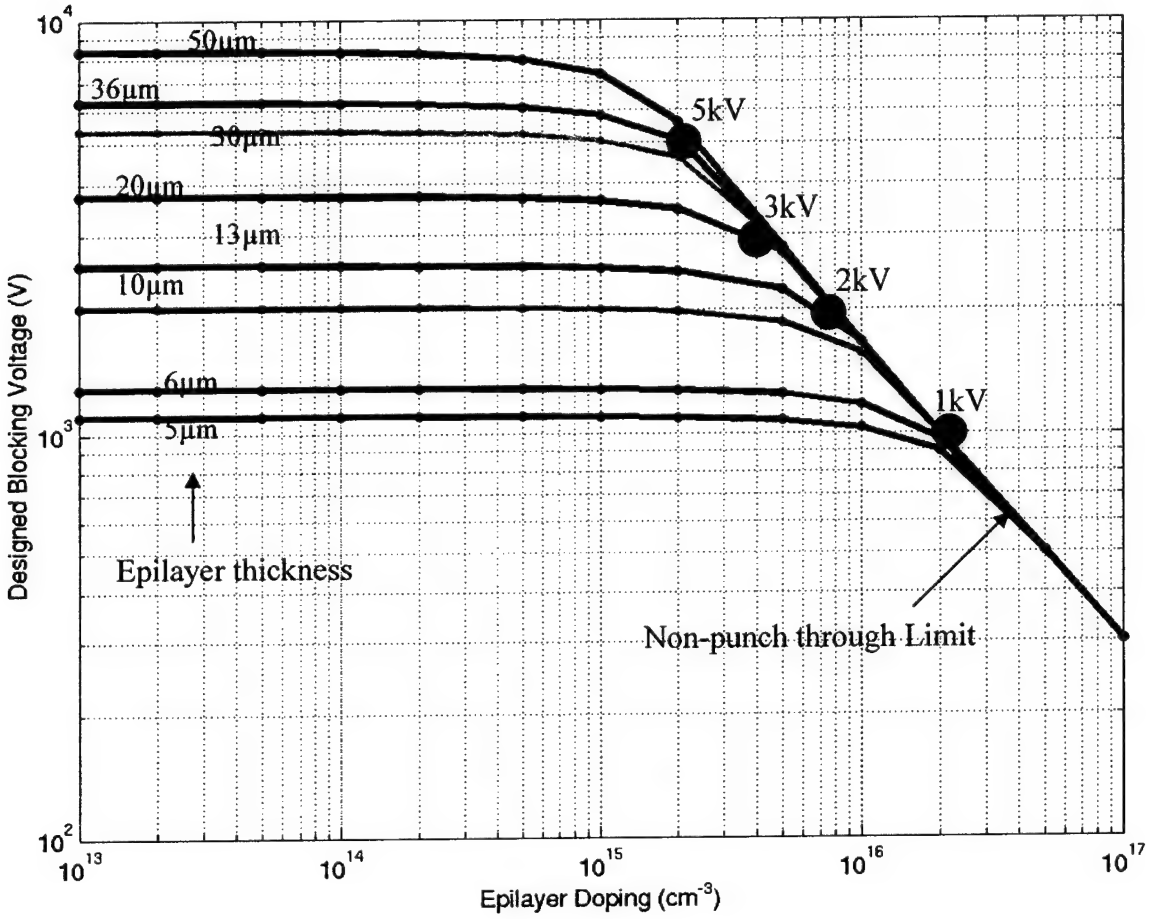


Fig. 5.4. 4H-SiC DMOS design chart showing breakdown voltage as a function of doping obtained by solving the ionization integral. Each line represents a different epilayer thickness and each circle represents the optimum drift region doping for a designed blocking voltage.

To calculate the resistivity ρ (Ω-cm) of the drift layer, the doping dependent mobility expressed by the Caughey-Thomas empirical relation [33] was used. The specific on-resistances were then calculated for JFET lengths of 4, 6 and 8 μm. The channel length was also varied from 3 to 0.5 μm. A contact resistance value of $\rho_c=1\cdot10^{-4}$ Ω-cm^2, an inversion channel mobility value of $\mu_{ch}=30$ cm^2/Vsec, a maximum oxide field of $E_{ox,max}=4$ MV/cm, a thickness of the p^+ base of $T_{base}=0.5$ μm, and a cell pitch of $S=5.5+L_{ch}+L_{JFET}/2$ μm were used in the calculations. The drift layer doping and thickness used in the spreadsheet calculations are summarized in Table 5.2.

Table 5.2

Designed Blocking Voltage (kV)	Drift Layer Thickness T_{epi} (μm)	Drift Layer Doping N_D (cm^{-3})
1	6	$1.7\cdot10^{16}$
2	13	$7\cdot10^{15}$
3	20.5	$4.2\cdot10^{15}$
5	36.5	$2.2\cdot10^{15}$

The $R_{on,sp}$ vs. designed blocking voltage plots for channel lengths of 3μm and 0.5μm are shown in Fig. 5.5 and Fig. 5.6 respectively. The source specific resistance calculated with a sheet resistance of 800Ω/□ is found to be higher than the JFET resistance for voltages below 2kV with $L_{JFET}=4$μm and for voltages below 3kV with $L_{JFET}=8$μm devices. The source resistance can be neglected for ≥3kV designs for both long and short channel devices.

For 3μm channel length devices, the resistance contribution from the channel proves to be very important, and a high channel mobility value is required for devices with designed blocking voltages ≤4kV. For short channel devices the channel resistance calculated with a $\mu_{ch}=30$ cm^2/Vsec is no longer the dominant resistance for ≥1.5kV designs.

As the designed blocking voltage is increased, the optimum doping of the drift region is decreased. The depletion region extension from the p^+ base into JFET region increases as the doping decreases, which pinches-off the JFET region and the $R_{JFET,sp}$ increases very rapidly for $L_{JFET}\geq4$ μm designs. $R_{DRIFT,sp}$ does not increase as rapidly as

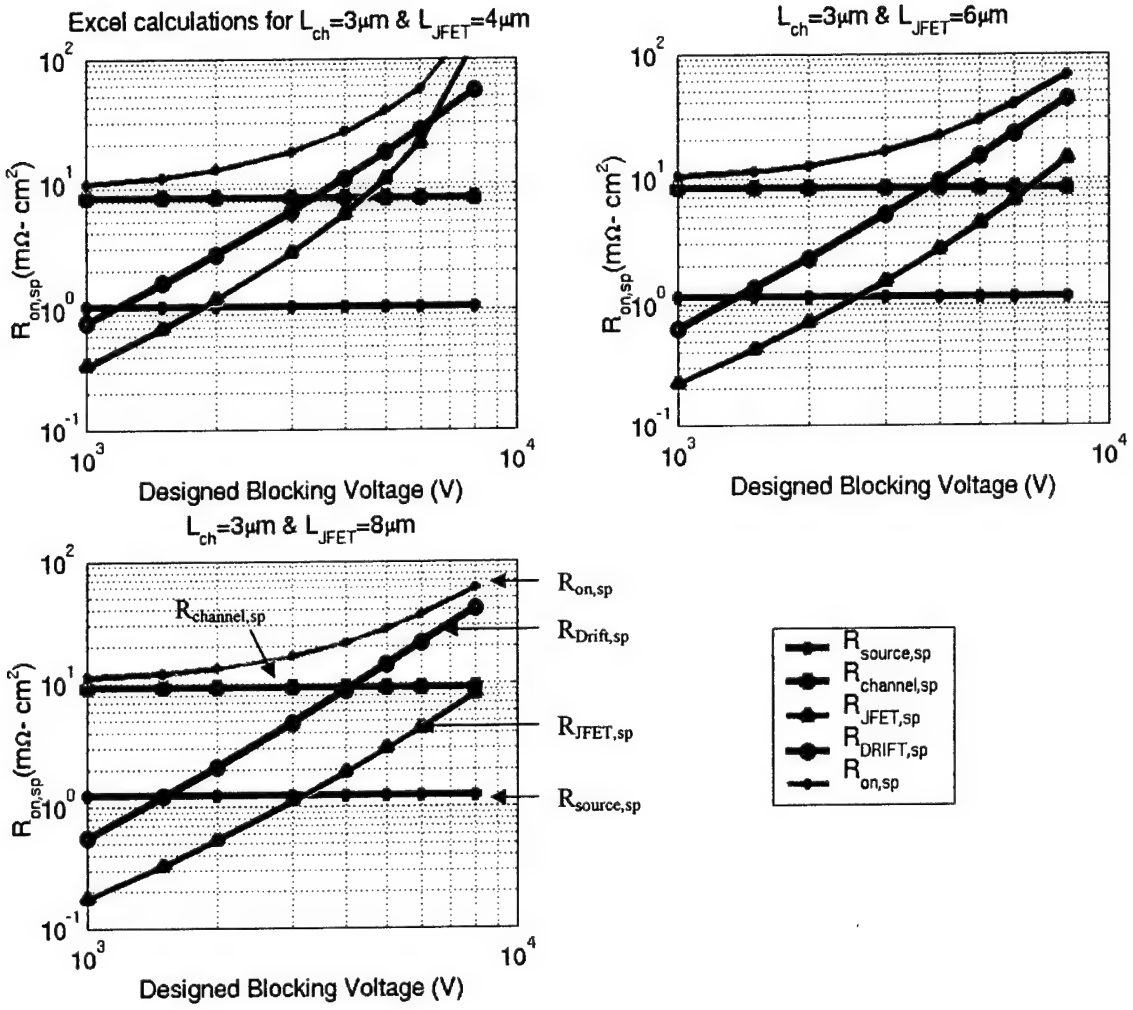


Fig. 5.5. EXCEL calculations of the specific on-resistances for the designed blocking voltagesfor a channel length of 3.0 μm.

$R_{JFET,sp}$ because as the drift layer doping is decreased with the increase in the designed blocking voltages, the drift layer thickness is also increased, and the current crowding is less for a fixed width. For L_{JFET}=4 μm, the cross-over point of the JFET and drift region resistances is at 6.3kV.

The blocking voltage values obtained numerically and the specific on-resistances calculated from the spreadsheet are only to be used as a design guideline. In the following section, MEDICI simulations are performed in order to verify our results obtained numerically. The breakdown voltages obtained from MEDICI simulations are less than those obtained numerically, as MEDICI takes into account the 2D electric fields within the structure.

5.4 MEDICI Simulation of the Short Channel DMOS Structure

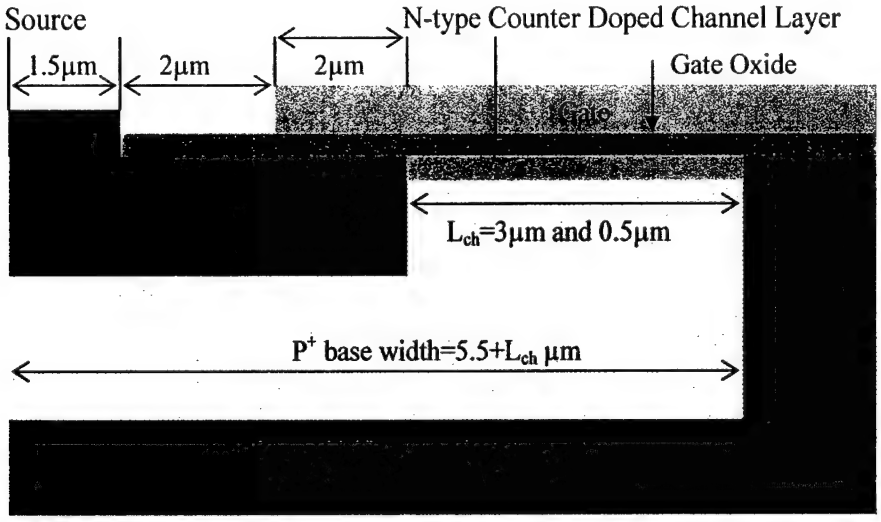


Fig. 5.7. Schematic cross-section of the MEDICI simulated structure.

MEDICI simulations were performed for the structure shown in Fig. 5.7 with a channel length of 3 μm and 0.5 μm. The drift layer doping and thickness used in the simulations are summarized in Table 5.3.

Table 5.3

Designed Blocking Voltages (kV)	Drift layer thickness T_{epi} (μm)	Drift layer doping (cm^{-3})
1	6	$2 \cdot 10^{16}$
2	13	$1 \cdot 10^{16}$
3	20	$4 \cdot 10^{15}$
5	36	$2 \cdot 10^{15}$

In order to obtain an optimum value for the JFET length, MEDICI simulations were performed on the structure with L_{ch}=0.5 μm, cell pitch S=6+L_{JFET}/2, and L_{JFET} of 2, 4, 6 and 8μm. The peak field in the oxide during the off (blocking) state was then calculated for 1kV, 2kV, 3kV and 5kV designs with the appropriate drift layer doping and thickness. The specific on-resistance values obtained from the EXCEL calculations performed in the previous section for a L_{ch}=0.5μm and channel mobility of 30 cm^2/Vsec were then plotted along with the peak field in the oxide for different JFET lengths for different device designs as shown in Fig. 5.8. The peak field in the oxide calculated from the MEDICI simulations is summarized in Table 5.4.

Table 5.4

Device Design	Applied Voltage (Volts)	Maximum Electric Field in the oxide (MV/cm)			
		L_{JFET}=2μm	4μm	6μm	8μm
1 kV	700	2.325	3.78	4.35	4.6
2 kV	1600	2.05	3.45	4.08	4.4
3 kV	2640	2.0	3.4	4.0	4.4
5 kV	4800	1.96	3.3	3.86	4.28

In the simulations, the maximum voltage applied is less than the designed voltage. The maximum allowable drain voltage for a device of a given epilayer thickness is chosen so that $E_{ox,max}$~4.5 MV/cm for an L_{JFET}=8 μm. This drain voltage is then used to

calculate E_{ox} for different L_{JFET}. The actual drain voltages used are tabulated in Table 5.4 The blocking voltage capability increases with the reduction in L_{JFET}, as the field in the oxide decreases.

In Fig. 5.8 as we go from 1kV to 5kV designed devices, the drift layer doping is decreased from $2 \cdot 10^{16}$ cm^{-3} to $2 \cdot 10^{15}$ cm^{-3} and the drift layer thickness is increased from 6 to 36 μm. The peak field in the oxide decreases with the decrease in doping for higher kV designs. For the 1kV design, L_{JFET} of 4 or 5 μm can be chosen to keep $E_{ox,max} \leq 4$ Mv/cm, and for 2kV design, $L_{JFET}=6\mu m$ can be chosen as the optimum JFET length, where the $R_{on,sp}$ is the minimum and $E_{ox,max}$ is close to 4 MV/cm. For the 3kV and 5kV device designs, the $R_{on,sp}$ minimum is at $L_{JFET}=8\mu m$ but the field in the oxide is around 4.2 MV/cm.

For MEDICI simulations of the specific on-resistances of long ($L_{ch}=3\mu m$) and short ($L_{ch}=0.5\mu m$) channel DMOS structures, a JFET length of 6μm was used. Figure 5.9 shows the simulated drain characteristics of a long and short channel DMSFET for 5kV design. The specific on-resistance was then calculated from the linear portion of the I-V plot.

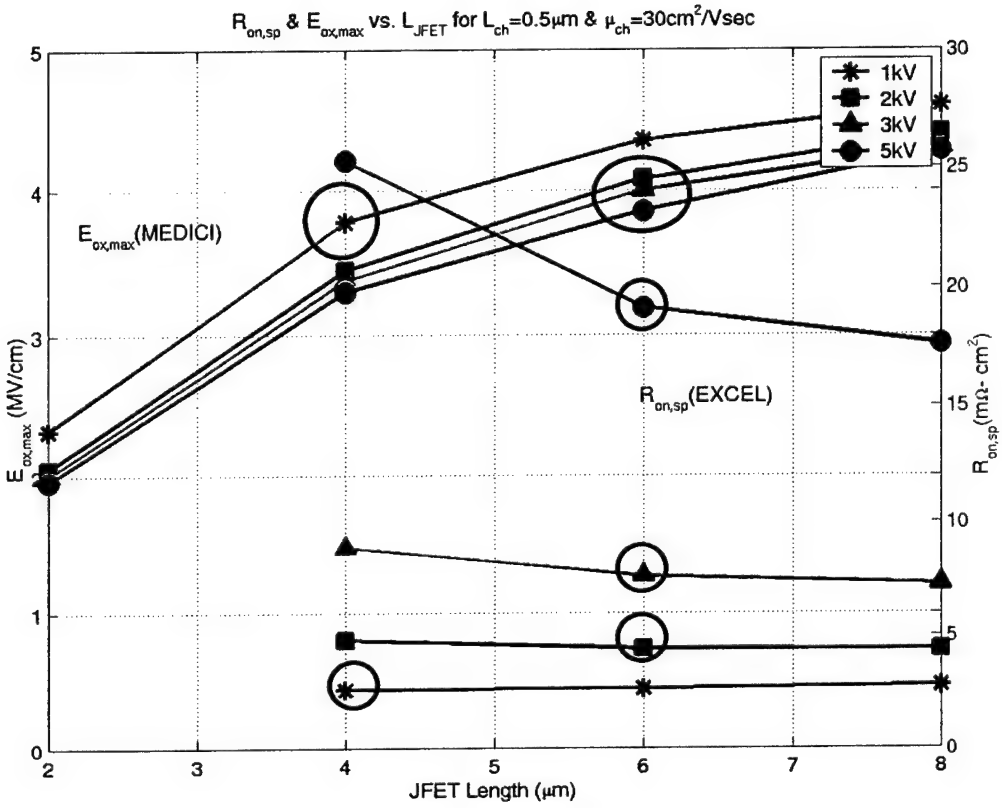


Fig. 5.8. Optimum JFET lengths for the short channel DMOS structure. Oxide electric field values for different designs are obtained from MEDICI simulations and the specific on-resistances are from EXCEL calculations. The black circles represent the optimum designed points for each BV curve keeping the oxide field $E_{ox} \leq 4$ MV/cm and the $R_{on,sp}$ at minimum .

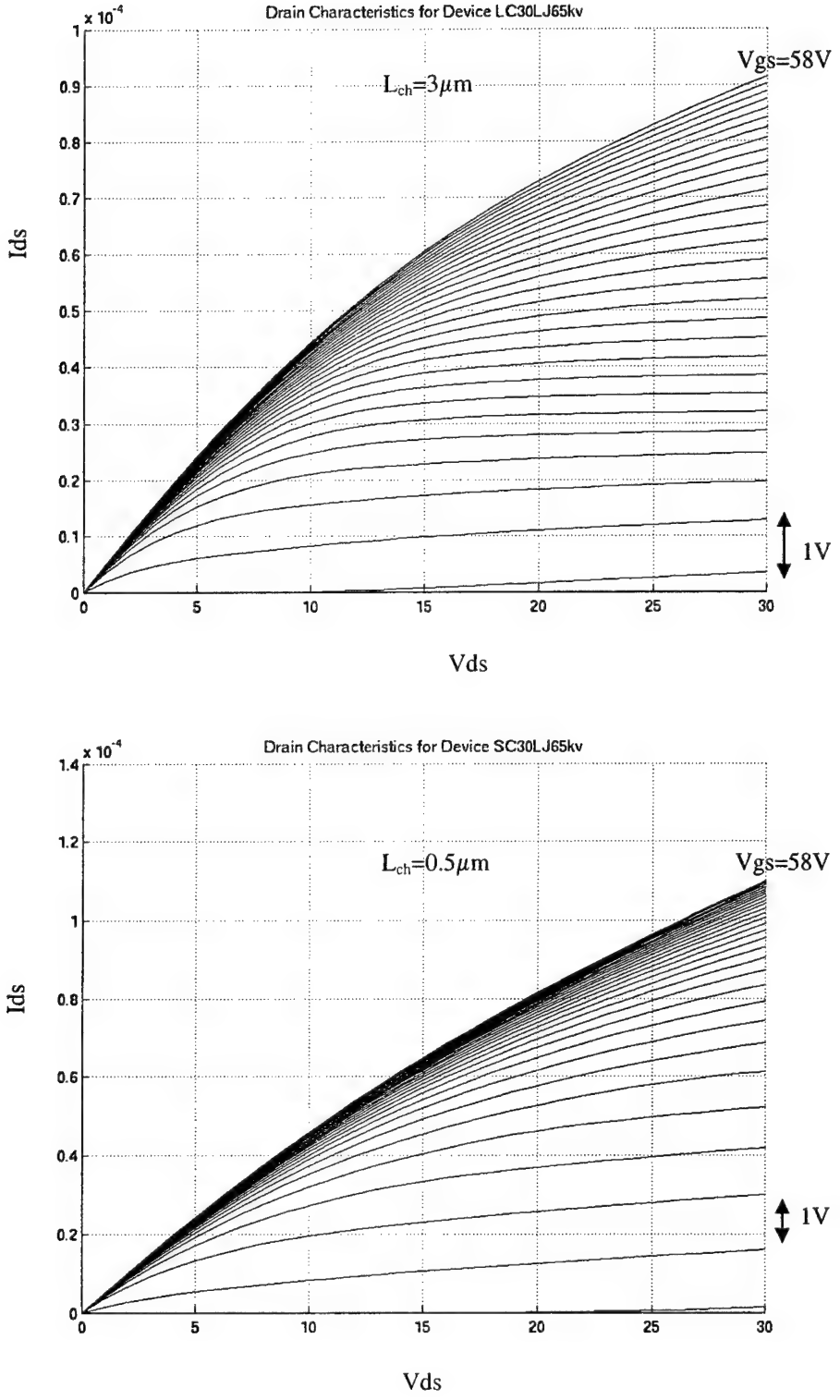


Fig. 5.9. Drain characteristics of a long and short channel DMOS structure for a 5kV design with L_{JFET}=6 μm and μ_{ch}=30 cm^2/Vsec.

Fig. 5.10 shows the summarized results for the short and long channel DMOS structure from EXCEL calculations and MEDICI simulations. The specific on-resistances obtained from MEDICI simulations agree well with that calculated from EXCEL. The slight discrepancies may be due to the fact that the drift layer doping and thickness are slightly different. Also, in the MEDICI simulations a buried channel region with $3 \cdot 10^{12}$ cm^{-2} dose was included to achieve the desired threshold voltage.

In conclusion, for the short channel DMOS structure, the specific on-resistance can be significantly improved with the reduction in the channel resistance. With appropriate drift layer doping and thickness, designed voltages blocking up to 8kV have been investigated with EXCEL calculations. The $R_{on,sp}$ vs. blocking voltage curve for L_{ch}=0.5 μm aligns with the 4H-SiC theoretical limit curve for high kV designs. This is because for high voltage devices, the drift region resistance dominates as the drift layer doping is reduced and the drift layer thickness is increased. The current crowing at the surface becomes less serious and the JFET resistance can be neglected. The reduction in specific on-resistance with a shorter channel length is more prominent for low kV designs. By reducing the channel length from 3 to 0.5 μm, the specific on-resistance can be lowered by a factor of 4 to 6 times with a 1 kV design as shown in Fig. 5.10. For higher kV designs, a shorter channel length may become as well important for situations, where the specific on-resistance is dominated by the channel resistance due to low inversion channel mobility values. Then, by making the channel length shorter, we can reduce the resistance contribution from the channel to the total $R_{on,sp}$. The EXCEL and MEDICI results are plotted at 70% of the designed blocking voltage, assuming actual breakdown voltage in a device with 2D field crowding at the edges will be lowered by 30%.

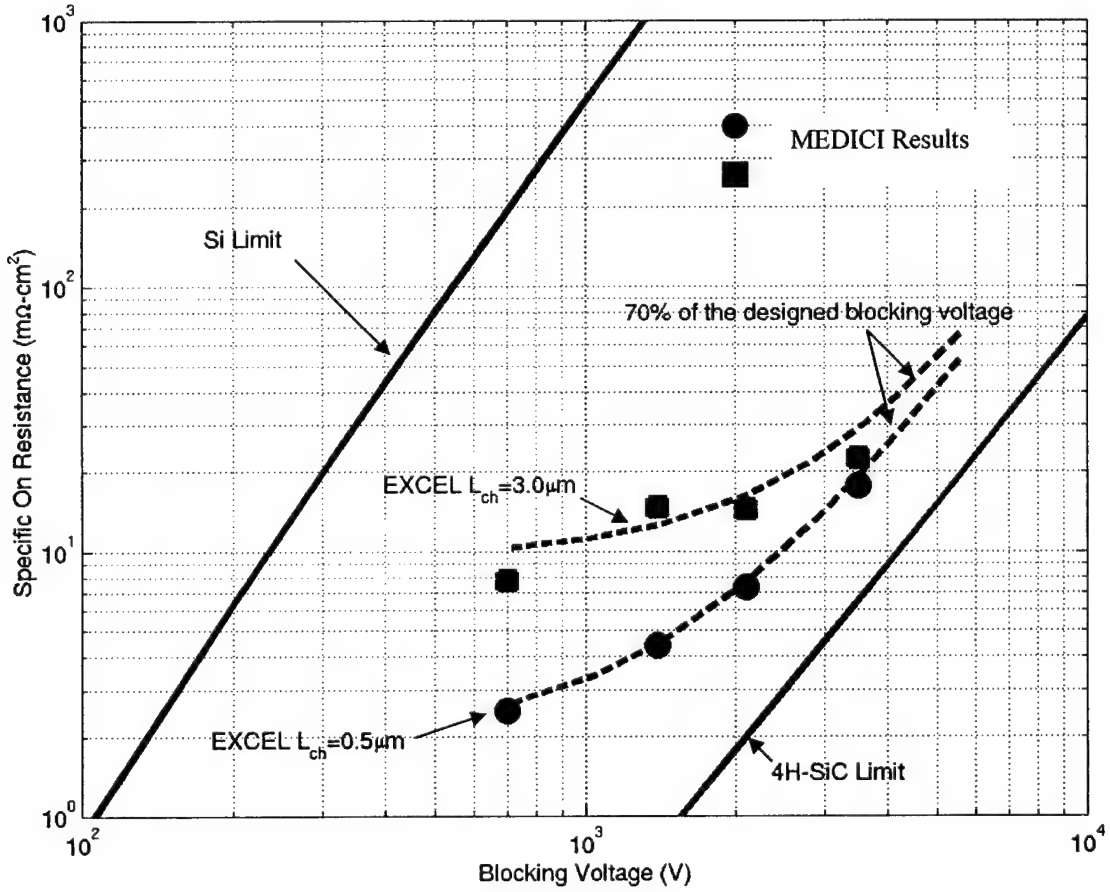


Fig. 5.10. EXCEL calculations and MEDICI results for the short and long channel DMOS structure.

6. PROCESS DEVELOPMENT OF A NOVEL COUNTER-DOPED SELF-ALIGNED SHORT CHANNEL 4H-SIC DMOSFET STRUCTURE

6.1 Motivation for a Counter-Doped Channel

4H-SiC DMOS transistors suffer from low values of inversion channel mobility when the channel is formed on implanted p-well regions, and the improvement of the MOS channel mobility is the focus of current research. Sheppard et al. [45] have demonstrated that the inversion channel mobility of a lateral MOSFET on 6H-SiC can be increased from 20 cm^2/Vsec to 140-180 cm^2/Vsec by implanting an n-type buried channel layer of $7.5 \cdot 10^{12}$ cm^{-2} dose. The channel mobility approaches the bulk channel mobility due to the implantation of the counter-doped layer. This idea was later applied to 4H-SiC power MOSFET structures where channel can be formed on an accumulation layer. Shenoy et al. [21] demonstrated the first 6H-SiC ACCUFET (Accumulation Channel FET) with a specific on-resistance of 18 mΩ-cm^2 and channel mobility value as high as 81 cm^2/Vsec. Later Tan et al. [11] demonstrated a 1400V 4H-SiC power UMOS ACCUFET with a specific on-resistance of 15.7 cm^2/Vsec, where the channel formed in an accumulation layer that was epitaxially grown.

6.1.1 An improved method for introducing a counter-doped channel in 4H-SiC DMOSFETs

ACCUFETs emerge as a possible solution for power MOSFETs on 4H-SiC due to the high channel mobility compared to the standard inversion mode MOSFETs. By introducing donor atoms of counter-doped implants, the negative charges of the acceptors at the p-type channel region are compensated, and the surface electric field can be reduced. The band bending at threshold condition is less with a counter-doped channel,

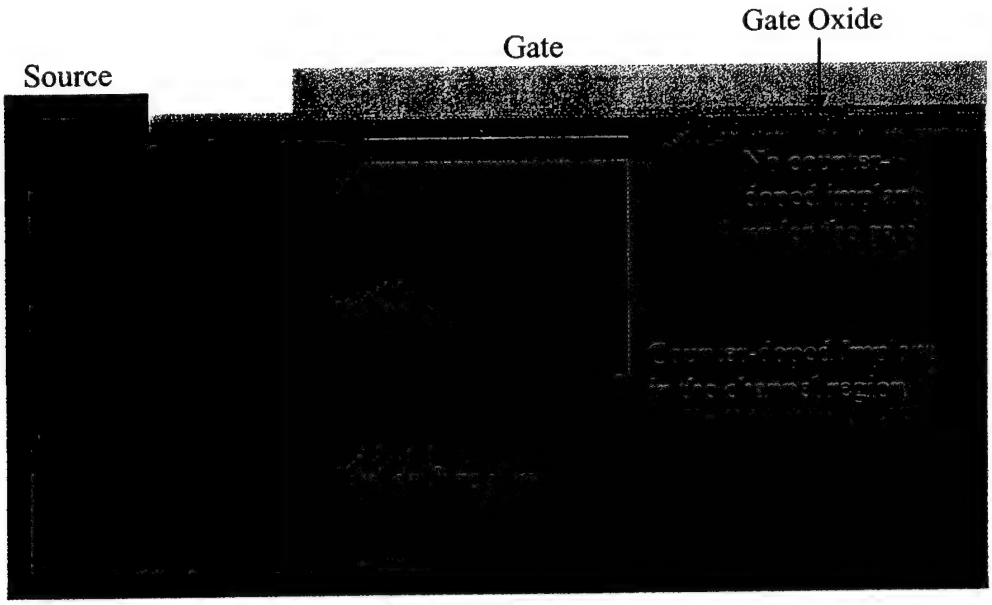


Fig. 6.1. An improved method of introducing counter-doped implantation

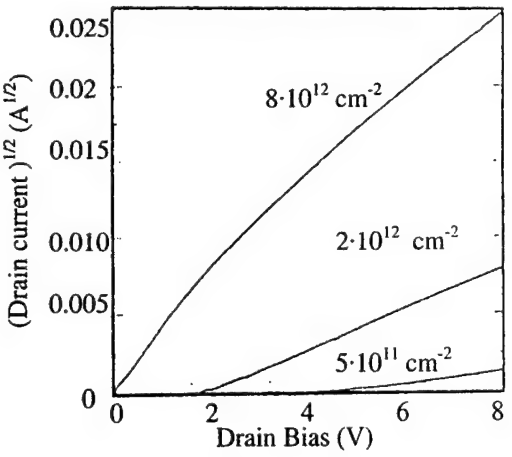
and the inversion charge density in the channel is increased. As the surface electric field is lowered, the channel mobility is improved, since the electron distribution is stretched away from the SiO_2/SiC surface, and surface roughness scattering is less with the counter-doped channel. The ionized impurity scattering is insignificant for surface inversion or accumulation layer due to carrier screening. The counter-doped implant improves the MOSFET threshold voltage and channel mobility, but unfortunately also lowers the blocking voltage capability. Most of the reported ACCUFET structures have the accumulation channel formed under the gate area between the JFET regions. For a power MOSFET structure, the blocking voltage is supported mainly across the lightly doped n^- drift region and heavily doped p-base region. As 4H-SiC material has eight times higher critical electric field than that of silicon, the gate is under high field stress during the blocking state. The field in the semiconductor increases with higher doping concentration in the JFET regions due to the counter doped implantation, and the oxide field is about 2.5 times greater than the field in the semiconductor ($E_{ox}=E_{SiC}\varepsilon_{siC}/\varepsilon_{ox}$) and can lower the breakdown voltage drastically by breaking down the gate oxide. Figure 6.1

shows a novel counter-doped DMOS structure. In this structure, the counter-doping implantation is only performed in the channel region and avoided under the gate area in the JFET regions. This can be achieved by performing the counter-doping implantation together with the p-well implantation using the same photo mask step. With this new method, all the benefits of the counter-doped layer in the on-state are preserved, while avoiding the disadvantages in the off-state.

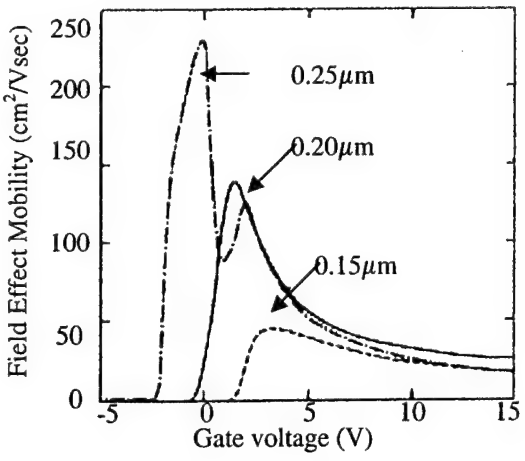
6.1.2 Thickness and dose consideration of the counter-doped implants.

The counter-doped implant reduces the threshold voltage and increase the channel mobility. Ueno el al [46] have investigated counter-doped 4H-SiC MOSFETs with different implant doses. FATFETs were fabricated on a $7.2 \cdot 10^{15}$ cm^{-3} p-type epilayer, and nitrogen S/D and counter-doped implants were activated at 1300^0C in argon for 30 min. The threshold voltage and shape and magnitude of the drain current have strong dependence on the implanted dose. As the dose is increased, the threshold voltage is decreased and the drain current is increased, and has a steeper turn on as shown in Fig. 6.2a. The field-effect mobility also increases dramatically with the implanted counter-doped dose. If the counter-doped dose is too high ($8 \cdot 10^{12}$ cm^{-2}), then the devices are normally on. With a recommended dose of $2.5 \cdot 10^{12}$ cm^{-2}, MOSFETs are enhancement type, and the mobility is higher than the best un-implanted mobility, as shown in Fig. 6.2b.

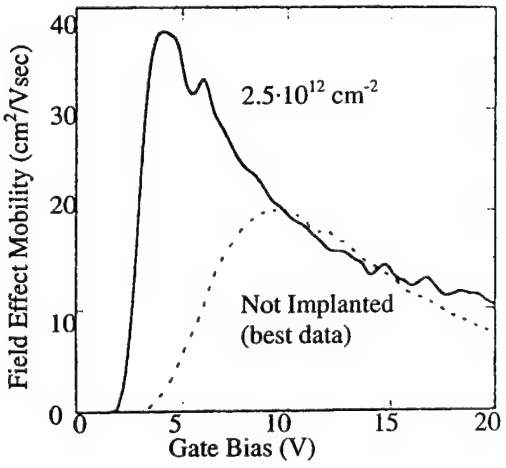
Harada et al [47] investigated the depth dependence of the counter-doped implant on the effective channel mobility. FATFETs were fabricated on a $5 \cdot 10^{15}$ cm^{-3} p-type epilayer with phosphorous S/D and nitrogen counter-doped implants, with a concentration of $1 \cdot 10^{17}$ cm^{-3} and depths of 0.15 μm, 0.2 μm, and 0.25 μm. All the implants were activated simultaneously at 1500^0C in argon for 5 min. Figure 6.2c shows that with a dose of $2 \cdot 10^{12}$ cm^{-3}, the low field mobility peak can be increased to 140cm^2/Vsec. The high field mobility then drops to 30 cm^2/Vsec at a gate voltage of 15 volts.



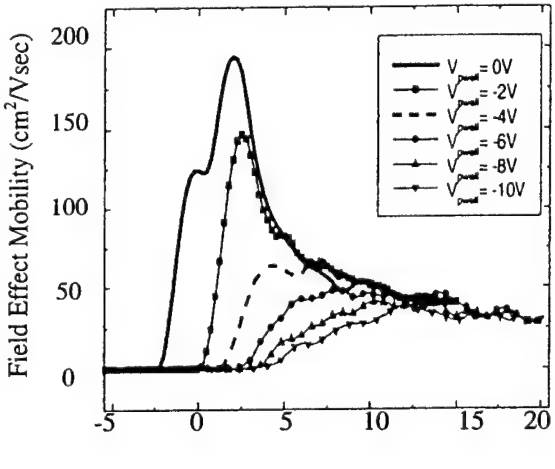
a) $\sqrt{I_D}$-V_D plot for different counter-doped nitrogen dose [46].



c) Field effect mobility for different counter-doped implant depth [47]. Dose=1·10^{12} cm^{-2} for all curves.



b) Field effect mobility with counter-dose of 2.5·10^{12} cm^{-2} [46]



d) Field effect mobility with counter-dose of 2.7·10^{12} cm^{-2} [48].

Fig. 6.2. Depth and dose selection of the counter-doped nitrogen implantation.

Ryu et al. of Cree Inc. [48] have demonstrated a buried channel DMOS structure with the MOS channel formed on aluminum-implanted p-wells in a 25 μm thick, $3 \cdot 10^{15}$ cm^{-3} n-type drift layer. All implants were activated at 1600^0C in argon with silicon overpressure. With a nitrogen counter-doped dose of $2.7 \cdot 10^{12}$ cm^{-2}, devices were normally on and showed a threshold voltage of -2 volt. Electrical measurements on the FATFETs yielded a high field-effect mobility peak of 194 cm^2/Vsec, which decreased to 25 cm^2/Vsec at a gate voltage of 20 volts, as shown in Fig. 6.2d. With -4 volts applied to the p-well, the device threshold voltage changed to positive 2.3 volts. Therefore, they recommend a dose of $(2.7 \cdot 10^{12} - 1.725 \cdot 10^{12}) = 1 \cdot 10^{12}$ cm^{-2} (where $\Delta Q = C_{ox} \Delta V$ = 6.9e-8 (F/cm^2) x 4.0(volt) /q = $1.725 \cdot 10^{12}$ cm^{-2}) in order to get a normally off device. It should also be noted that the counter-doped implantation significantly improves the low-field mobility, but the high field mobility drops to 30 cm^2/Vsec at the operating gate voltage of 20 volts.

The accumulation channel mobility is higher than the inversion channel mobility because the minority carriers are distributed near the SiO_2/SiC interface, and as the band bending is less, they are less affected by the fixed charge and interface states. At low field the mobility is determined by the Coulomb scattering due to charge centers and phonon scattering [49]. At high fields, mobility is governed by surface roughness scattering [49]. In low field regions, the accumulation channel mobility increases with gate field due to carrier screening and also due to the spatial distribution of majority carriers away from the interface. At high fields, the accumulation layer mobility approaches (drops to) the best reported inversion layer mobility due to surface roughness scattering.

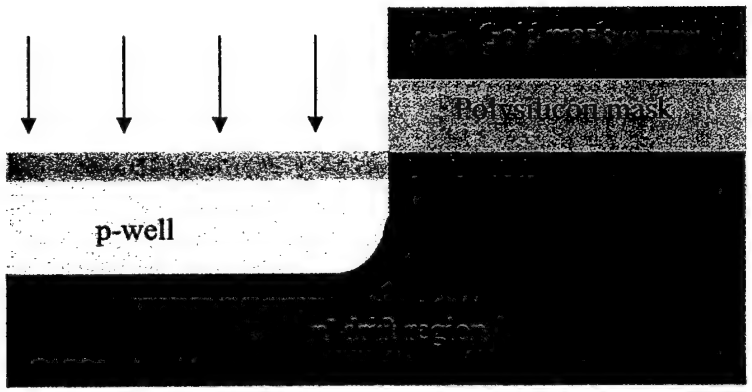
6.2 A Novel Process for Self-Aligned Base and Source Regions in 4H-SiC DMOS Structures

The 4H-SiC power DMOS structure suffers from low inversion channel mobility, and the best reported mobility value on implanted p-base regions is still below 30 $cm^2/Vsec$ at the maximum allowable field of 4MV/cm, even incorporating counter-doping implantations to improve MOS mobility. Thus, the channel resistance of the power MOSFET structure dominates the total specific on-resistance. The channel length in the DMOS structure is lithographically defined by the alignment tolerance between the base and source implant masks, and is limited to 2 to 3 μm using conventional optical lithography. With a shorter channel length, the specific on-resistance can be readily lowered by a factor of 5 to 6 times in addition to other methods of improving the MOS channel mobility. We now describe a novel self aligned process that enables us to obtain a channel length ≤0.5 μm. The process steps are outlined below, making reference to Fig. 6.3.

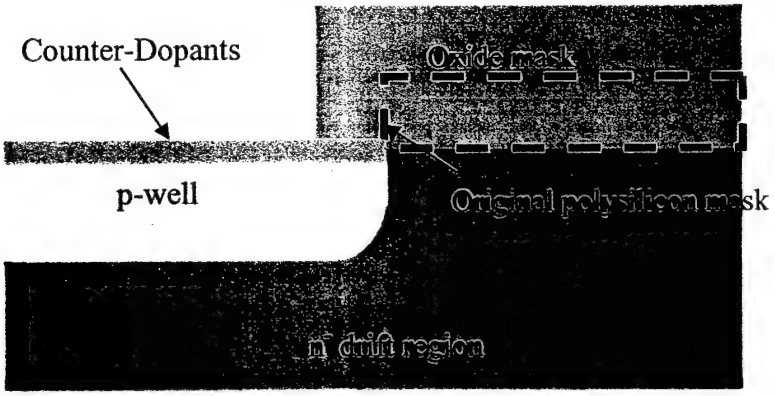
1) First a 0.5 μm thick polysilicon layer is deposited and patterened with a Ni/Au/Ti (0.15μm/0.5μm/0.02μm) layer, to serve as an implant mask for the p-type base implantation. The counter-doping implantation is performed at the same time. Figure 6.3a shows the device cross-section at this stage.

2) The metal mask is removed and the polysilicon layer is thermally oxidized to get 1.0 μm thick oxide, which serves as the source implant mask. Figure 6.3b shows the device cross-section.

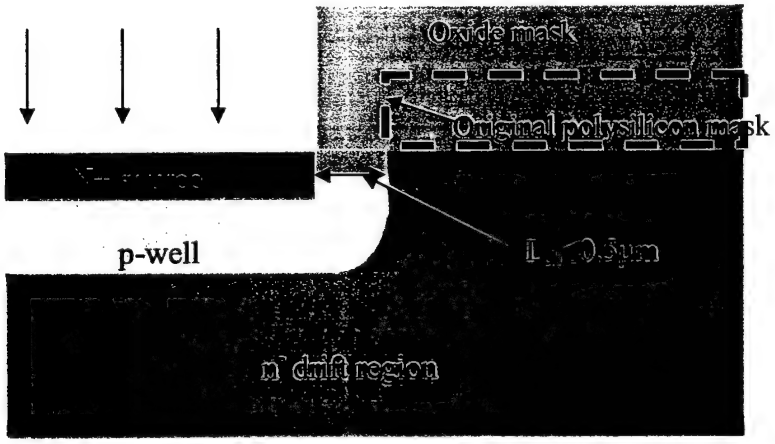
3) Source implantation is performed with the oxide mask, which has a lateral displacement relative to the p-type base implant mask by about 0.5 μm and this defines the channel length. Figure 6.3c shows the device cross-section at this stage.



a) p-well implantation



b) Oxidizing polysilicon mask



c) Source implantation

Fig. 6.3 Process steps for the self aligned base and source regions.

6.3 Experiments Performed to Obtain Vertical Side Wall Spacers

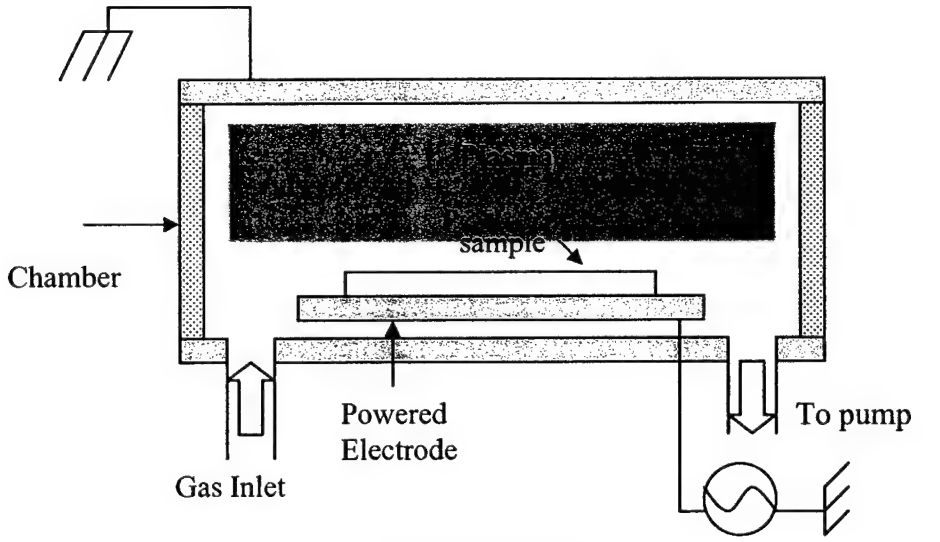
The oxidation of polysilicon gates in LDD (lightly doped drain) structures to form sidewall spacers is widely used in silicon process technology. The same idea was used in this experiment to obtain oxide side wall spacers, which allowed source regions to be self-aligned with respect to the p-base. By controlling the polysilicon oxidation temperature and time, a channel length of ≤ 0.5 μm can be obtained.

I. POLYSILICON DEPOSITION

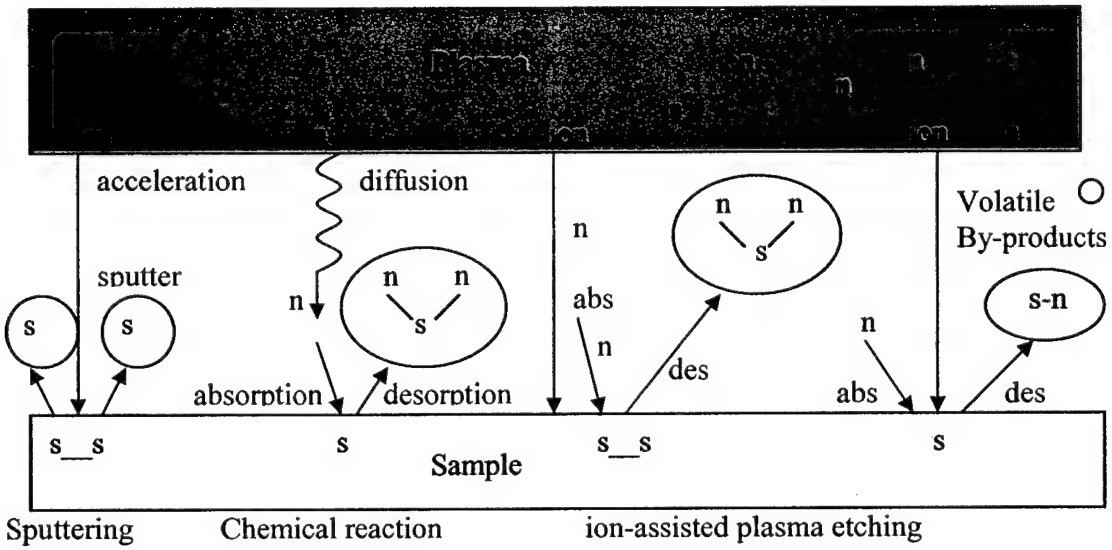
Polysilicon was deposited on two 6H-SiC test pieces by LPCVD of silane (SiH_4) at a temperature of 600^0C for 1hr 40min and for 2hr 45min, which resulted in polysilicon thickness of 0.88 μm and 1.56 μm respectively. The deposition rate of polysilicon showed an exponential dependence on temperature. The deposition temperature was limited to 600^0C, as the deposited film showed smoother surfaces compared to the films grown at temperatures higher than 600^0C. At 600^0C temperature the deposition rate is slow and measured to be about 90 to 95A^0/min.

II. RIE OF POLYSILICON

The reactive ion etching system at Purdue is a TTL RIE80, manufactured by Oxford Plasma Technology. The TTL RIE80 is a parallel plate etcher with 300W RF power. The RIE (reactive ion etching) system consists of an etching chamber, a vacuum pump, an RF power supply, and etchant gases as shown in Fig. 6.4a. In RIE, the sample is placed inside the chamber in which etchant gases are introduced. A plasma is formed using an RF power supply, which emits a characteristic glow of the etchant gas. The plasma contains chemically reactive species like atoms, radicals (for example, $SF_6+e \rightarrow SF_6^*$ is an excited state of SF_6, and is electrically neutral but highly reactive), and



a) RIE system setup



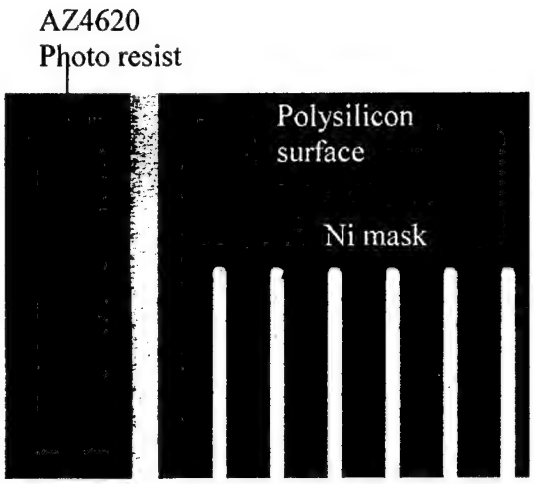
b) Etching Mechanisms

Fig. 6.4. A simple parallel-plate reactive ion etching system.

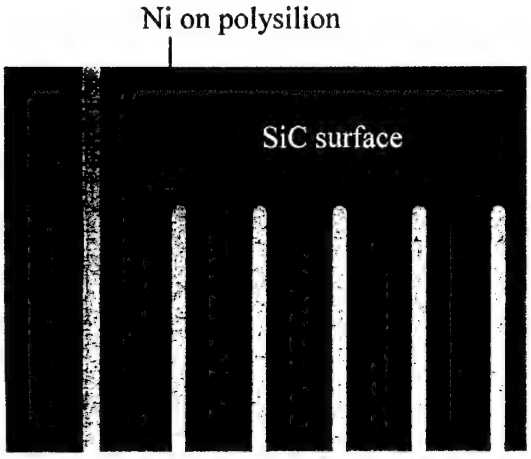
ions ($e+SF_6 \rightarrow SF_6^+ +2e$) etc. These reactive species then diffuse to the surface of the material being etched. The etching process can take place by 1) spontaneous etching, where a chemical reaction takes place and volatile by-products are desorbed from the surface and diffuse into the bulk of gas; 2) energetic ion-assisted etching, where spontaneous etching take place in the direction of ion bombardment as the ion induced damage increases the surface's reactivity; and 3) sputtering etching, where ions impart enough energy to knock atoms off the surface. Once the plasma is formed, the electrons are swept toward the powered electrode and thus a negative dc bias with respect to the plasma is formed. If the pressure inside the chamber is reduced, the electron mean free path is increased, and more electrons go to the powered electrode and increase the DC bias further. Now, created ions can strike the sample surface with higher energy, and the etching process is sputtering (anisotropic). If the etching action is purely chemical, then the etching process can be of an isotropic nature.

In this experiment the polysilicon layer was patterened by pure SF_6 (sulfur hexafluoride) gas. With fluorine based plasmas, the fluorine atoms etch polysilicon isotropically, and hence anisotropic etching of polysilicon with SF_6 is difficult. The channel length of the DMOS structure will depend on the degree of sidewall taper, and thus a high degree of anisotropy is required in addition to high uniformity of etching. The ability to achieve anisotropic etching is dependent on the high energy ion bombardment of the fluorine atoms. In this experiment, to achieve a vertical sidewall profile, the etching parameters investigated were, RF power and DC bias (pressure is inversely proportional to the DC bias). Silicon test samples were RIE etched at high and low DC bias value at 30, 75, and 100 watts of RF power. The etch rate of silicon increased with increased power, as expected, and with high DC bias of 350 to 380 volt, a more anisotropic etch of silicon was achieved compared to that with a low bias values of 220 to 250 volts. SEM (scanning electron microscopy) was used to examine the etched samples.

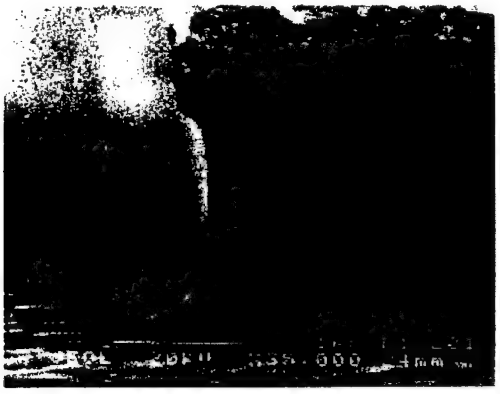
The deposited polysilicon on the two 6H-SiC test pieces were patterned with a nickel mask transferred by liftoff lithography. The mask used was designed for the p-well implantation of the DMOS structure consisting of long fingers, as shown in Fig. 6.5a. Figure 6.5b shows the fingers after RIE etch of polysilicon. The etch rate was between



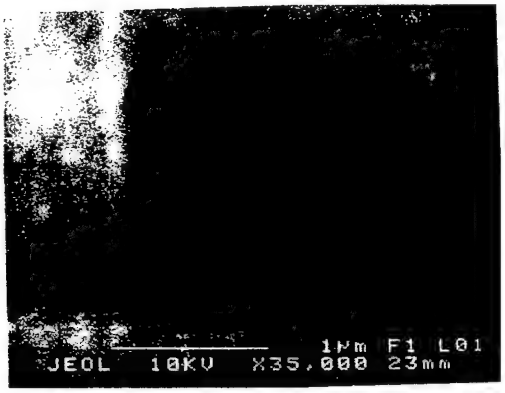
a) Mask pattern used for RIE experiments



b) After polysilicon etch by RIE



c) SF_6 gas, 100W power and 360V DC bias sidewall etch profile of polysilicon.



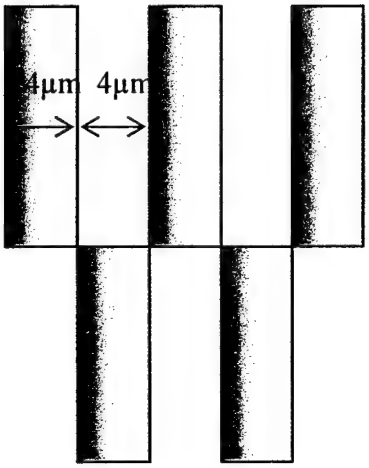
d) SF_6 gas, 100W power and 390V DC bias sidewall etch profile of the polysilicon.

Fig. 6.5. Experiments performed to obtain a vertical side wall profile on the RIE etched polysilicon layers. With higher DC bias we get more anisotropic etch of the polysilicon layer.

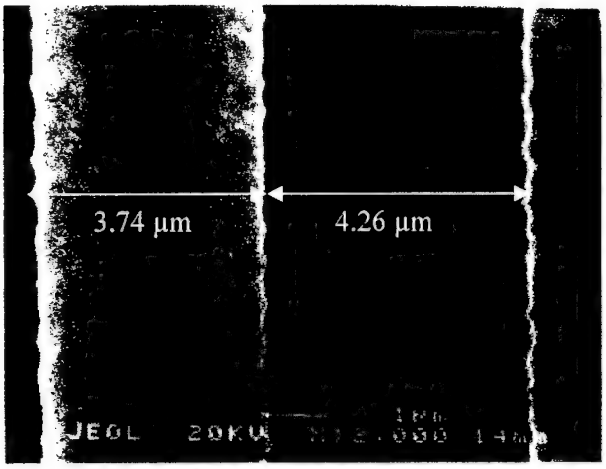
900 to 1000A^0/min. In order to avoid micro masking of nickel during the RIE process, the nickel mask was covered with AZ4620 positive photoresist with a DF (Dark Field) mask specially made for this purpose. The two SiC test samples were then RIE etched at 100 watt power in SF_6 gas, with 10 sccm flow rate at a DC bias of 360 volts. Figure 6.5c shows the SEM picture of the sidewall of the patterned polysilicon layer. Another (6H-SiC) test piece was later etched at a 380 to 400 volts DC bias with other process parameters kept the same, and the resulting sidewall picture is shown in Fig. 6.5d. Thus, as pressure is lowered, the self bias (DC bias) is increased, bombarding ion energies are larger, and we get more sputtering etching which results in a vertical sidewall, even with pure SF_6 gas.

III. OXIDATION OF POLYSILICON

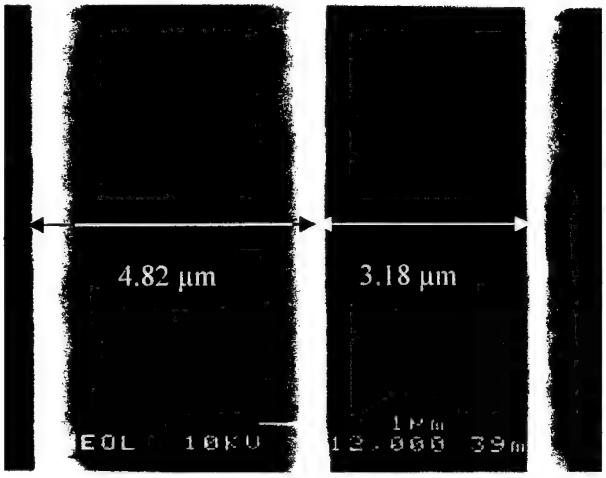
After the polysilicon etching, the etch mask was removed from the two 6H-SiC samples and the etch depth measured with a Tencor Alpha Step profilometer were 0.88 and 1.56 μm. The mask used contained some alignment features with fixed widths, as shown in Fig. 6.6a and b, which were used to determine the channel length. SEM pictures were taken before and after the polysilicon oxidation. By measuring how much the gap between each feature closed up, we can estimate the distance between the edge of the oxide sidewall and the original polysilicon mask. The polysilicon oxidation was performed at a temperature of 1000^{0}C in wet O_2 in order to minimize any oxidation of unannealed p-type implants in real devices. Figure 6.7 shows the oxide thickness for wet undoped poly oxidation at various temperatures [50]. The polysilicon needed to be oxidized for 6 hrs in order to get an oxide thickness of 1.2 to 1.3 μm, as estimated from Fig. 6.7.



a) Patterns used to measure the oxide sidewall spacers.



b) SEM picture of alignment marks before oxidation.



c) SEM picture of alignment marks after 6 hrs of oxidation.

Fig. 6.6. Experiments performed to obtain side wall spacers 0.54μm away from the original polysilicon mask.

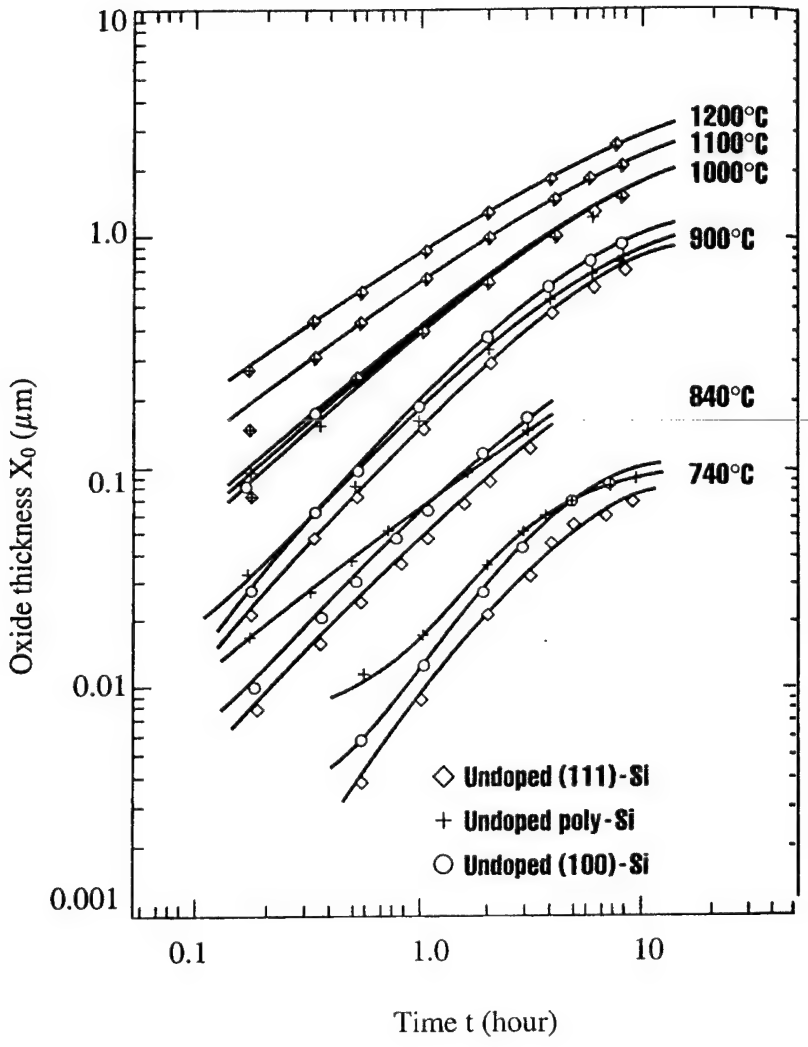


Fig. 6.7. The oxidation of undoped polysilicon in wet ambients [50].

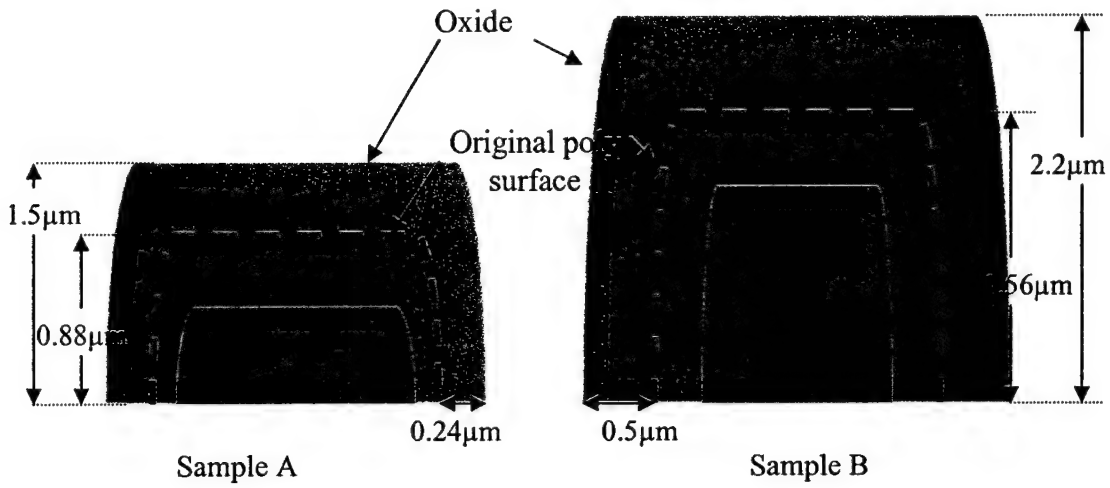


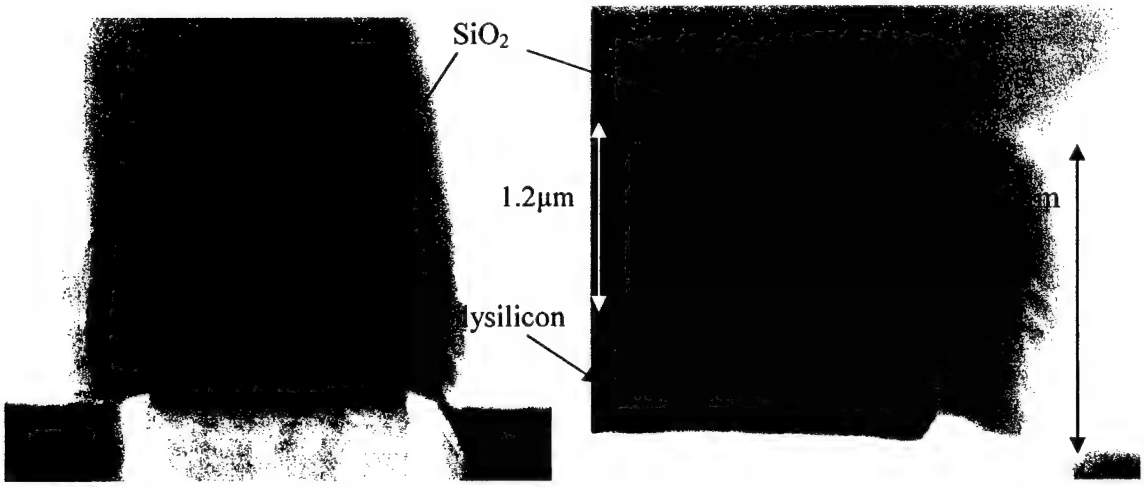
Fig. 6.8. Oxide thickness calculations after the 6 hr poly oxidation of the two 6H-SiC test samples.

The oxide will expand 54% above and 46% below the original polysilicon surface. The two 6H-SiC test pieces were then re-measured after the oxidation step, and the resulting thicknesses were 1.5 μm (oxide plus unoxidized poly thckness for sample A) and 2.2 μm (sample B) respectively (see Fig. 6.8). The resulting oxide thicknesses were t_{ox}=(1.5-0.88)/0.54=1.15 μm and (2.2-1.56)/0.54=1.18 μm respectively. A thin layer of gold (30A^0) was then deposited and SEM photographs of the alignment marks were taken. Figure 6.6c show alignment marks after the polysilicon oxidation step.

Polysilicon oxidation rate depends on grain orientation, dopant type, and dopant concentration. Lightly doped polysilicon oxidizes in wet O_2 at a faster rate than silicon, and heavily-doped polysilicon oxidizes more rapidly than undoped polysilicon [51]. In this experiment, the etched polysiliocn fingers and unetched poly surface showed two different oxide colors indicating two different oxide thicknesses as shown in Fig. 6.9a. In addition to this, the polysilicon fingers showed two different oxide thicknesses on the vertical and lateral surfaces. The oxide thickness on the etched sidewall was smaller than that on the top surface. From the experiment we find that even though oxidizing the two samples simultaneously resulted the same oxide thicknesses on the top surfaces, sample

A yielded a sidewall spacer of 0.23 to 0.24μm, and sample B showed a sidewall spacer of 0.5 to 0.54 μm, due to the dependence of the oxidant diffusion on the shapes of the surfaces [52]. Figures 6.9c and d show two different oxide thicknesses on the polysilicon fingers. To achieve a channel length ≥0.5 μm, in the final device processing 1.5 to 1.6 μm thick polysilicon mask should be used, and after 6 hrs of oxidation the total thickness (poly-oxide+unoxidized poly) should be ≥2.2 μm.

a) Nomarski microphotograph of the two different polysilicon oxidation thicknesses. The edge oxide color was "pink" and everywhere else the poly-oxide color was "blue".



b) SEM picture of the cross-section of the polysilicon fingers after oxidation. Magnification x12000, 10KV

c) SEM picture of oxide sidewall spacers. Magnification x22000, 10KV

Fig. 6.9. Two different oxide thicknesses were observed during the oxidation of the patterned polysilicon layer. The polysilicon finger oxide color was pink and oxide in the unpatterned polysilicon area was blue. In addition, the vertical and lateral oxide thicknesses on the fingers were also different. The oxide on the top surface was 1.2 μm and on the side wall was about 1.0 μm.

6.4 Punch-Through Simulations

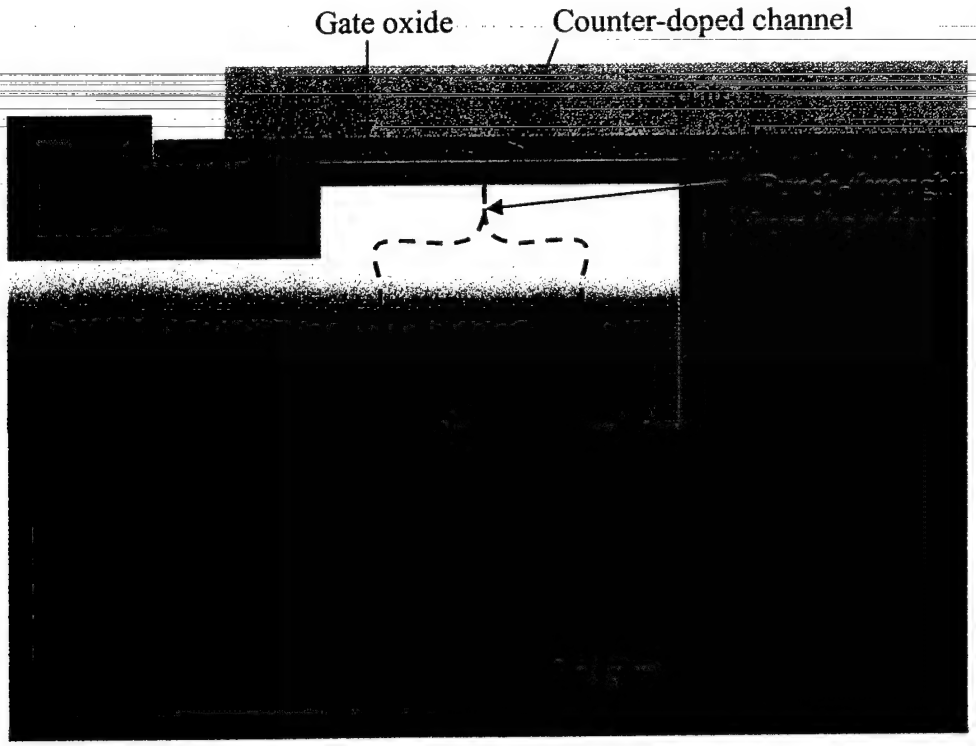


Fig. 6.10. Schematic cross-section of the counter-doped DMOS structure showing "punch-through" condition. Here, the shaded area represents the retrograde doping profile in the p-type base region, and the blue dotted line represents the depletion region edges at reverse bias condition.

Selective doping in SiC is accomplished by ion implantation, due to small diffusivity of impurities at temperatures below 1800^0C, and also due to unavailability of a suitable mask layer at this high temperature. The fabrication of DMOS (Double Implanted) transistors requires a p-type base implantation and an n-type source implantation. The p-type base implantation usually has a retrograde profile, where a low doping concentration near the surface results in a low threshold voltage, and a higher doping concentration near the p-base and n^- drift junction blocks high voltages during the off-state. During the blocking mode, the p-base, the source, and the gate all are grounded

and a positive voltage applied to the drain extends the depletion region mainly into the lightly doped n^- drift region. The reverse voltage is supported across the heavily doped p^+ and lightly doped n^- junction. Due to low doping of the p-channel region, a depletion region can also extend into the p-channel region (see Fig. 6.10). A punch-through condition is reached when the depletion region of the n-type drift layer "punches-through" to the n^+ source either from the side or from the bottom. In this situation the reverse voltage can no longer be supported, as electrons flow from the source to the drain through the p-base. The critical electric field value at avalanche breakdown for a drift doping $N_D=4\cdot10^{15}$ cm^{-3} (3kV design) is equal to $2.2\cdot10^6$ V/cm (see Fig. 1.1 for 4H-SiC material). The doping concentration (N_A) and thickness (X_p) product of the p-base region must be $N_AX_p=\varepsilon_sE_{CR}/q=1.2\cdot10^{13}$ cm^{-2} to prevent this "punch-through" condition. With a channel length of 0.5 μm, the doping of the p-type channel must be $2.4\cdot10^{17}$ cm^{-3} to prevent punch-through from the side. With this high p-channel doping the threshold voltage will be high, and a counter-doped channel implant can be used to lower the threshold voltage. In this section, MEDICI simulations are performed on a 3kV DMOS design to see the effect of counter-doping on the breakdown voltage. The simulated structure is shown in Fig. 6.11.

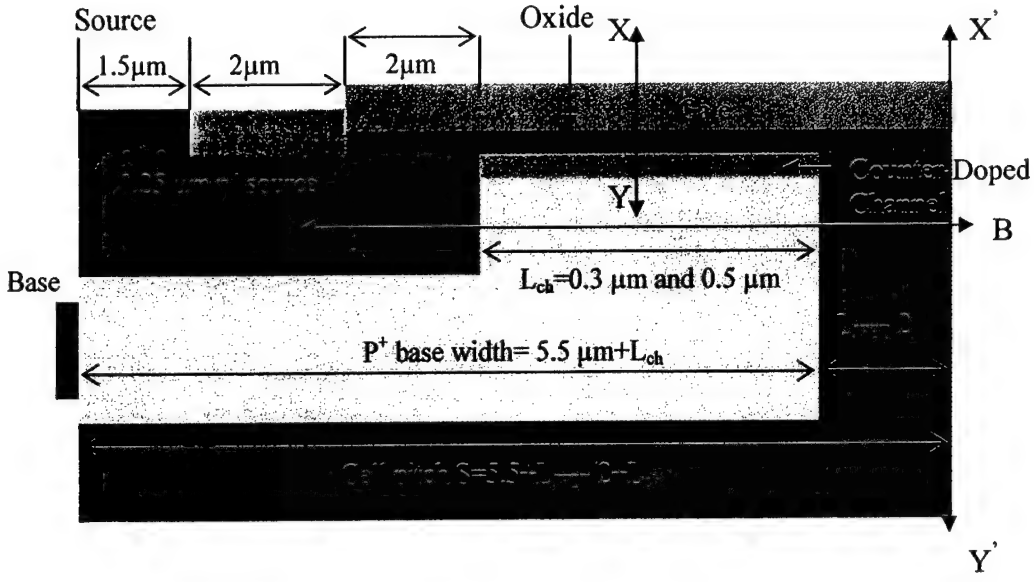


Fig. 6.11. Structure used for "punch-through" MEDICI simulations.

For a 3kV design, a drift layer doping of $2.5 \cdot 10^{15}$ cm^{-3} and thickness of 20 μm was used. A retrograde p-type doping of $2.5 \cdot 10^{17}$ cm^{-3} in the channel region and $1 \cdot 10^{18}$ cm^{-3} in the base region was used. For a 0.5 μm channel length and L_{JFET}=6μm, counter-doped doses (Q) of $1 \cdot 10^{12}$ cm^{-2}, $2.72 \cdot 10^{12}$ cm^{-2}, $3.4 \cdot 10^{12}$, cm^{-2} and $5 \cdot 10^{12}$ cm^{-2} were investigated. Figure 6.12 shows the doping profile at X↔Y for a counter-doped dose of $3.4 \cdot 10^{12}$ cm^{-2}. After compensation, the surface is n-type with a doping of (N_D-N_A=$3.4 \cdot 10^{17}$ cm^{-3}-$2.5 \cdot 10^{17}$ cm^{-3}=$9 \cdot 10^{16}$ cm^{-3}) ≈$1 \cdot 10^{17}$ cm^{-3}. With the application of a 2600V reverse voltage to the drain, the electric field profile at X'↔Y' and A↔B were inspected. Figure 6.13 and 6.14 shows the electric field at the gate (X'↔Y') and across the n^+ source-p-base-n^- JFET (A↔B) junctions respectively. The oxide electric field is 3.59 MV/cm at 2600 V. From Fig. 6.13, 0.2 μm of undepleted p-channel region (2.6 μm≤ x ≤2.8 μm) ensured "no-punch-through" at this counter-doped dose.

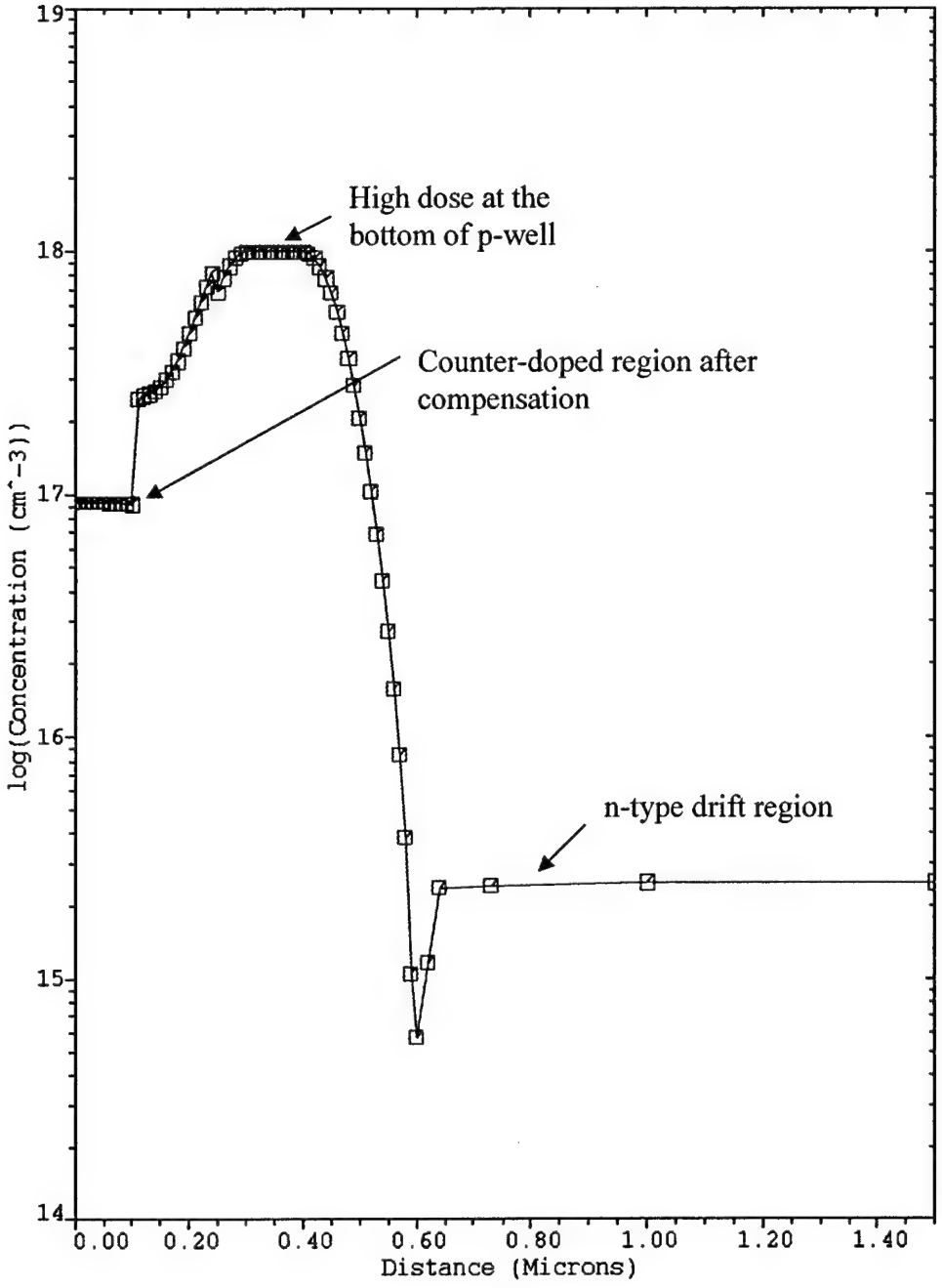


Fig. 6.12. The retrograde p-well doping profile used in MEDICI simulations.

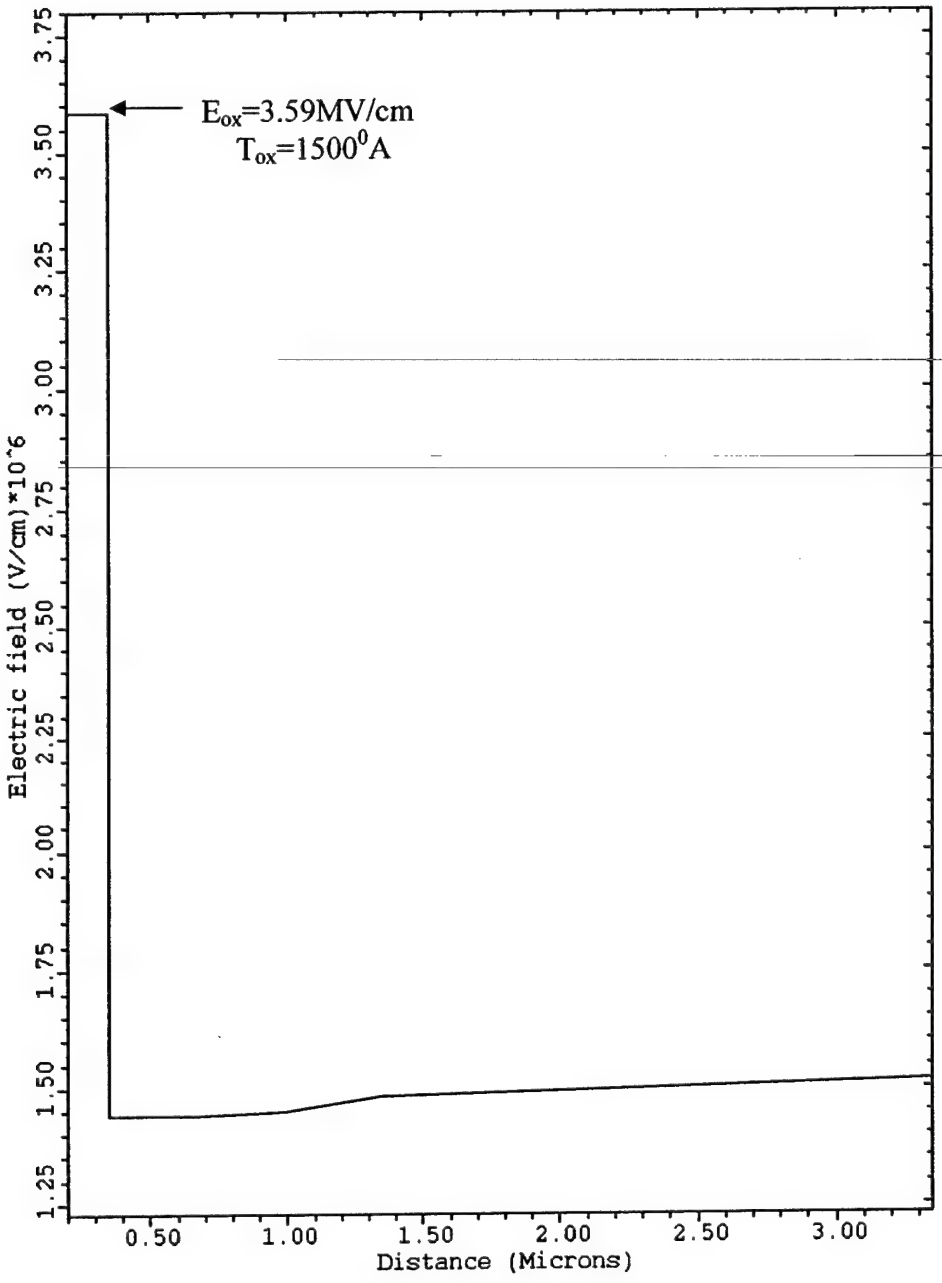


Fig. 6.13. Electric field profile across the gate oxide along line X'↔Y' at 2600V drain voltage.

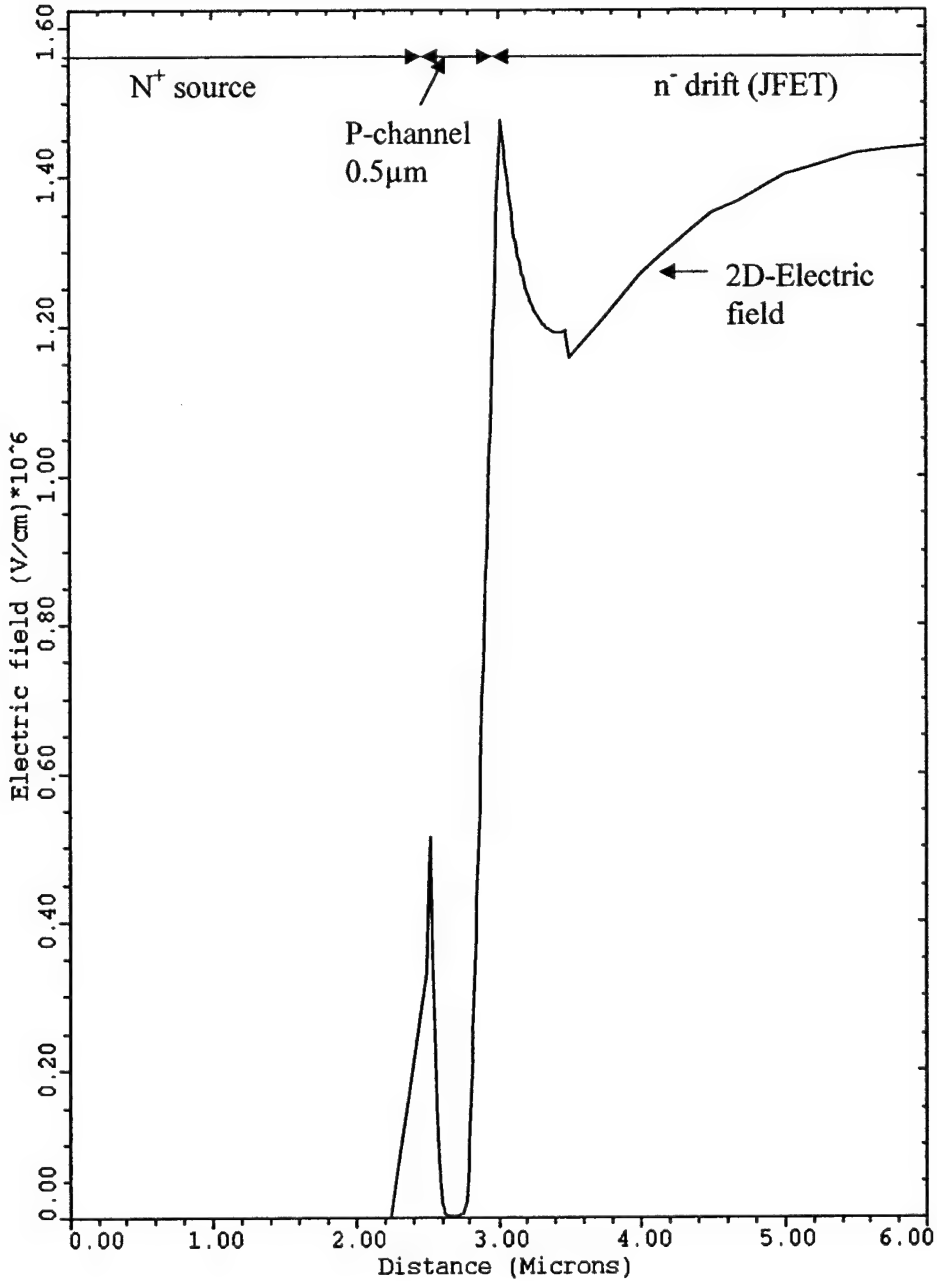


Fig. 6.14. Electric field plot across the n^+ source-p channel-n^- JFET region along line A'↔B' with 2600V applied to the drain.

Figure 6.15 shows the leakage current (A/μm) through the device for the different counter-doped doses ($1 \cdot 10^{12}$ to $5 \cdot 10^{12}$ cm^{-2}), and it is clear that the structure does not "punch-through" for a channel length of 0.5μm. Later, the channel length was decreased to 0.3 μm and with a dose of $1 \cdot 10^{12}$ cm^{-2} the device could still block 2600V (see Fig. 6.16). However, with Q=$2.72 \cdot 10^{12}$ cm^{-2} and Q=$3.4 \cdot 10^{12}$ cm^{-2}, the "punch-through" condition is reached at a voltage of 700V (I=1mA/cm^2) and 1200V (I=1mA/cm^2) respectively. The blocking capability could then be increased to 2400V and 2200V respectively with the application of a negative gate voltage of -6V as shown in Fig. 6.16.

From the simulations we conclude that with a channel length of 0.5 μm there is no punch-through with p-channel doping of $2.5 \cdot 10^{17}$ cm^{-3}, if the counter-dose is kept $\leq 5 \cdot 10^{12}$ cm^{-2}. As we decrease the channel length to 0.3 μm, there is still no punch-through if the counter-doped dose is kept $\leq 1 \cdot 10^{12}$ cm^{-2}.

6.5 A Self-Aligned Source and Base Contact Process in 4H-SiC DMOS Structure

Figure 6.17 shows two types of source and base contacts for the DMOS structure. Figure 6.17a is the non-self aligned contact, where a 2 μm alignment tolerance is kept between the source and base contacts. The cell pitch is then $S=9.0+L_{ch}+L_{JFET}/2$ for this structure. If the aluminum contact to the p-type base region is placed adjacent to the nickel contact to the n^+ source region, then the alignment tolerance of 2 μm is eliminated and the cell pitch for the self-aligned contact reduces to $S_{self\text{-}aligned}=7.0+L_{ch}+L_{JFET}/2$, as shown in Fig. 6.17b. By reducing the cell pitch we can reduce the area of the device and thereby reduce the specific on-resistance of the device. For process simplification, the nickel contact to n^+ source is allowed to go over the aluminum contact to the p-type base.

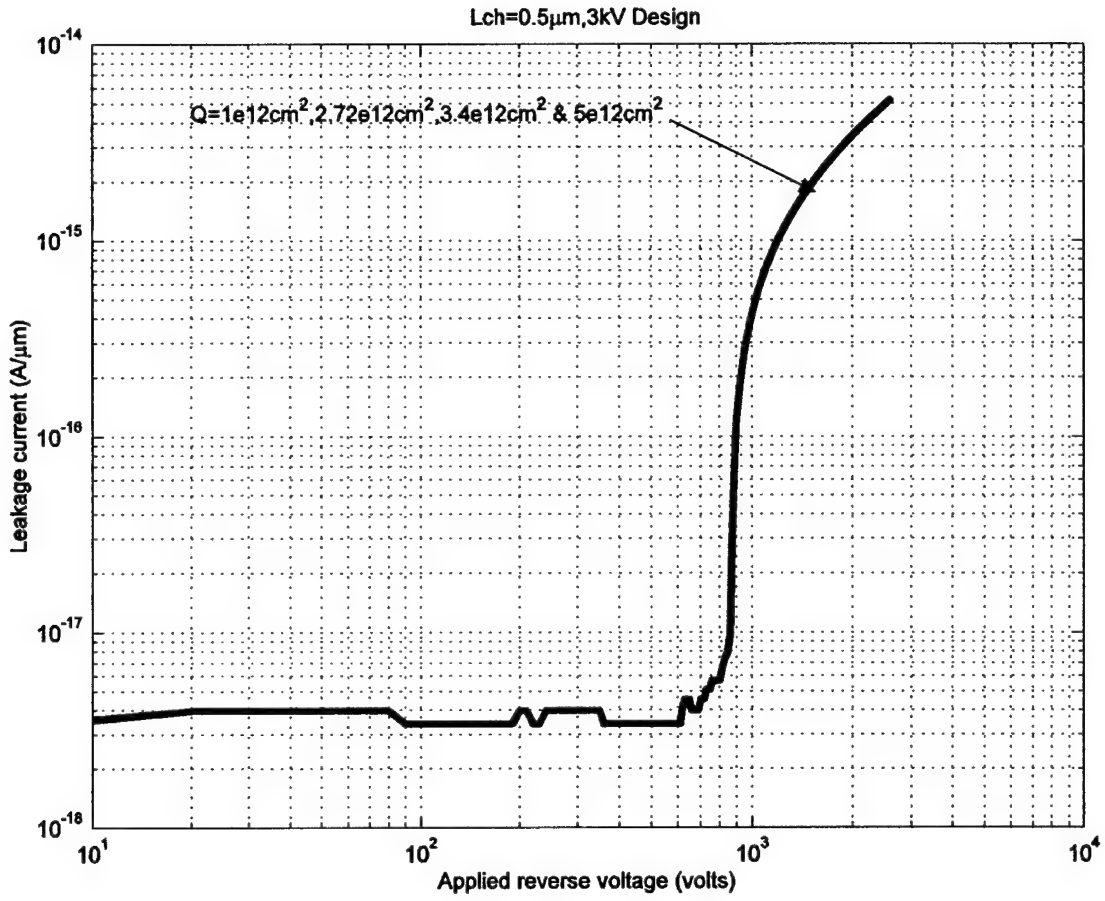


Fig. 6.15. Punch-through simulations of leakage currents for a channel length of 0.5μm and with different counter-doped dose.

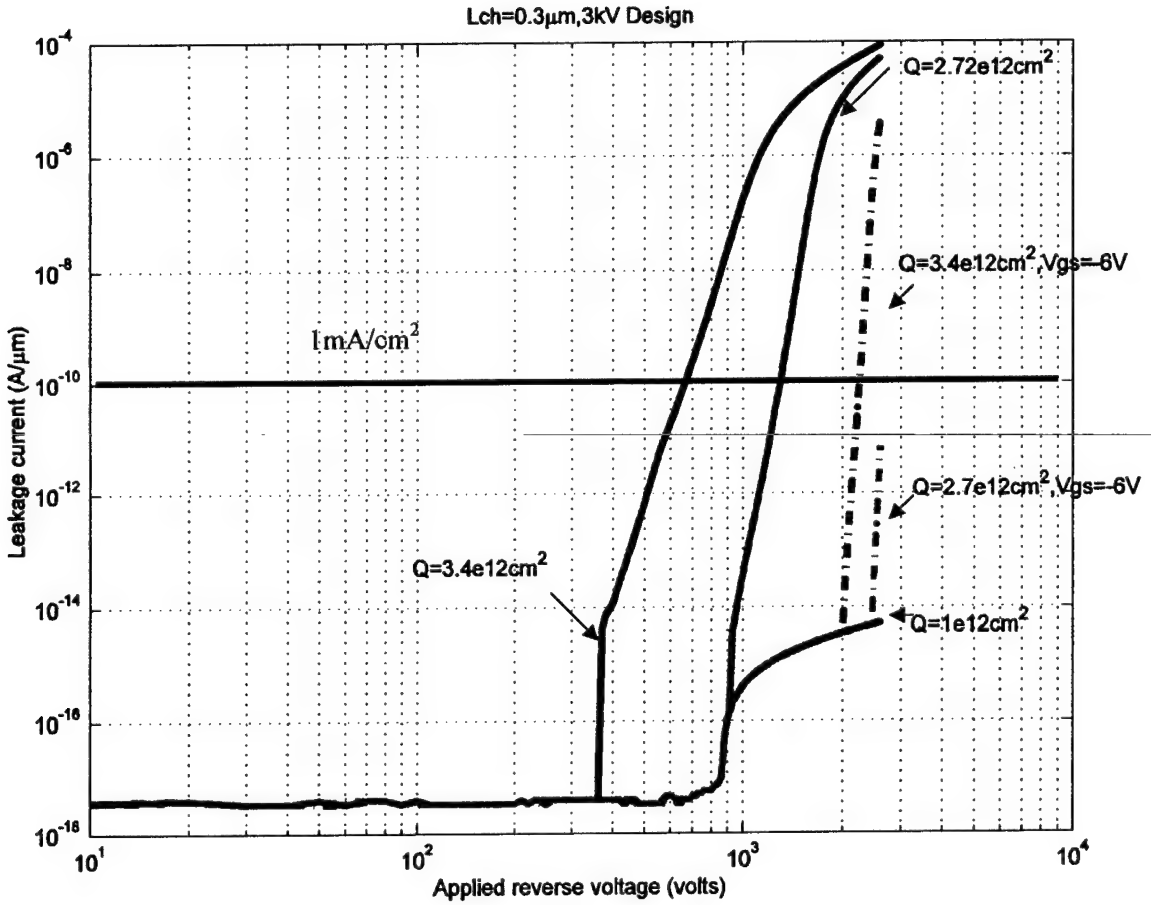
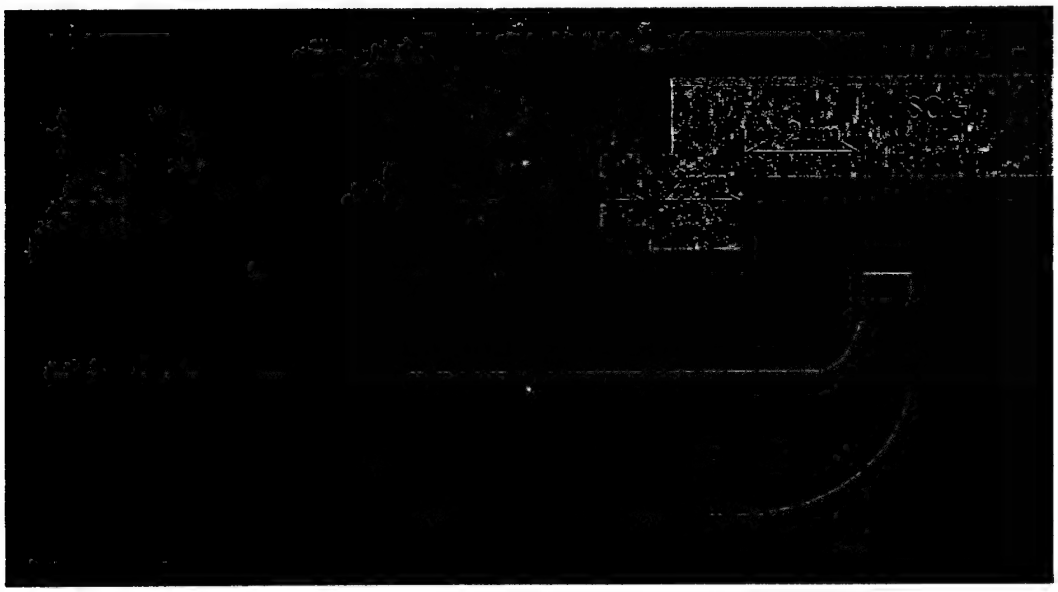
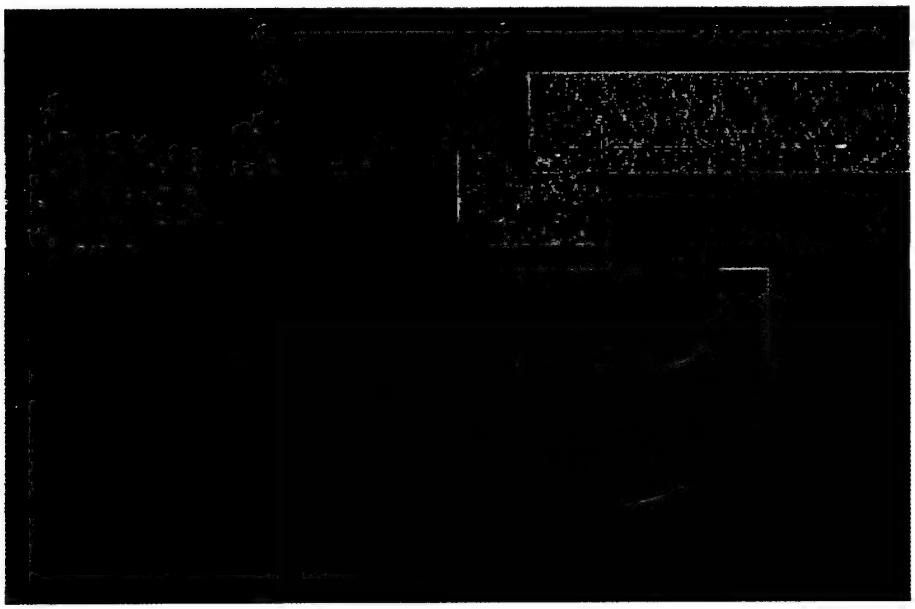


Fig. 6.16. Punch-through simulations of leakage currents for a channel length of 0.3μm for different counter-doped dose. Solid curves are with V_g=0 and dashed curves are with Vg=-6V.



a) Non self-aligned source and base contact



b) Self-aligned source and base contact

Fig. 6.17. A self-aligned source and base contact in the DMOS structure.

A detailed experiment was performed to investigate the effect on contact resistance of the p-type SiC when the nickel layer was allowed to go over the aluminum layer. The process steps are outlined as follows:

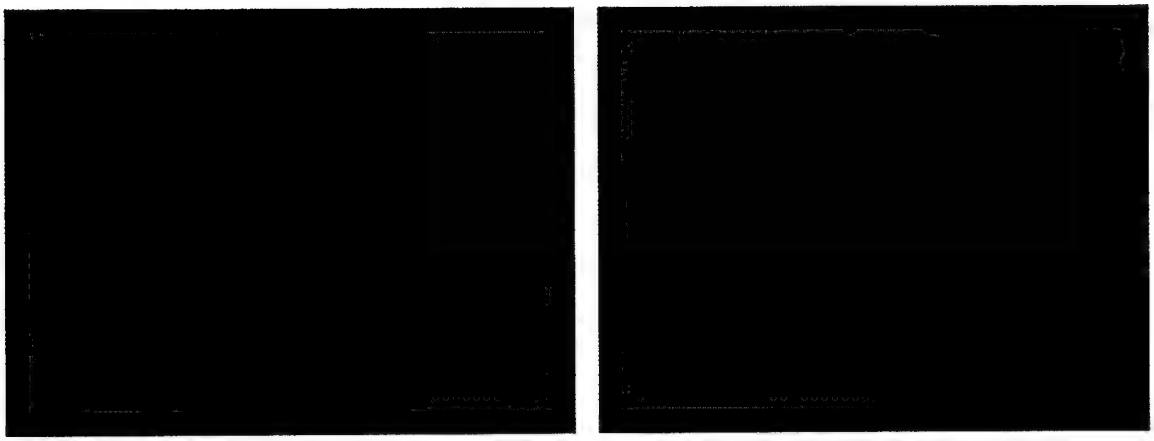
Step #1: TLM structures were formed on $1.1 \cdot 10^{19}$ cm^{-3} doped p^+ epilayer, 2 μm thick 6H-SiC material. To isolate the TLM structures, a p^+ trench etch was performed by RIE of SiC at 100W, in SF_6 gas for 70min. $2000A^0$ of nickel was e-beam deposited and liftoff lithography process was used to form the RIE mask. The etch was performed at a low DC bias to prevent micro-masking of nickel. Alpha-step measurements gave the etch depth as 2.39 μm.

Step #2: The 6H-SiC sample was then cut in half with a diamond scriber. $500A^0$ of aluminum was deposited on both pieces, and on one piece, $375A^0$ of nickel layer was deposited on top of the aluminum layer. Figure 6.18a and b shows a photograph of the samples after the metal deposition.

Step #3: Both the pieces were annealed in vacuum at 1000^0C for 2min. Figures 6.18c and 6.18d show the TLM structures after the contact anneal.

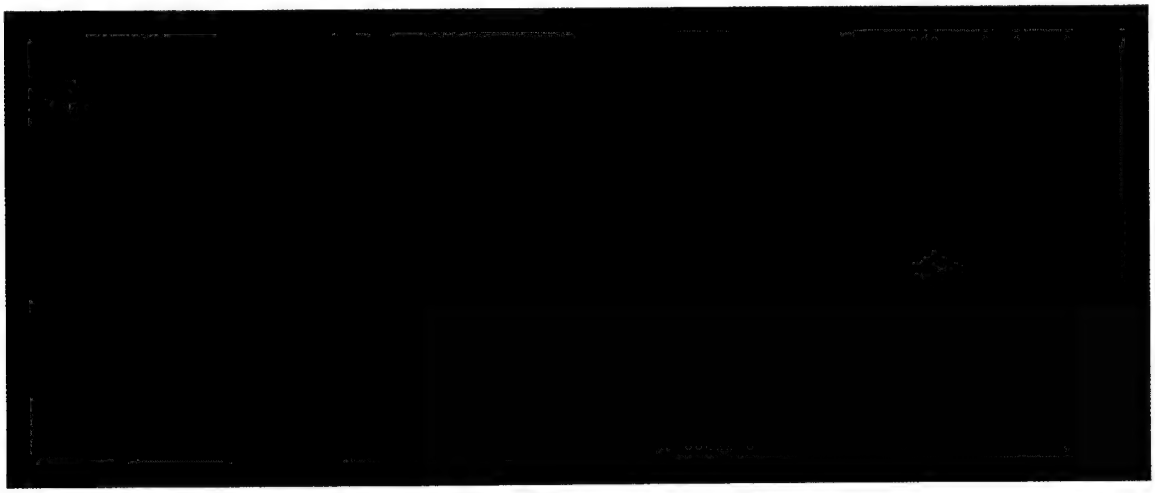
Step #4: Finally, $550A^0$ of aluminum was deposited as top metal by liftoff lithography.

The TLM structures with only aluminum metal showed a rougher surface compared to the piece with nickel covering the aluminum layer. This is because at 1000^0C, aluminum is at liquid phase and once melted, has a tendency to form aluminum balls as shown in Figure 6.18d. The Al-Ni is about 30/70 [$500A^0$(Al)/$375A^0$(Ni)] weight %. I-V characteristics of the TLM contacts were not ohmic, but the current levels for the contacts with nickel over aluminum were three times higher compared to the aluminum contact. TLM measurements were taken near the origin where the I-V curve looked linear. The lowest specific contact resistance value obtained from the aluminum contact



a) Ni plus Al metal contact before anneal, magnification x500.

b) Al contact before anneal, magnification x500.



c) Ni plus Al metal contact after anneal at 1000^0C for 2 min at vacuum. Magnification x500.

d) Al contact after 1000^0C anneal. Note the surface appears rough after contact anneal. Magnification x500.

Fig. 6.18. Experiments performed on self-aligned source and base contact.

and from the nickel over aluminum contact was $9.8 \cdot 10^{-4}$ Ω-cm^2 and $2.8 \cdot 10^{-4}$ Ω-cm^2 respectively. With the self-aligned source and base contact deposition process, we can reduce the cell pitch and at the same time obtain a low contact resistance to the p-type base region.

7. FABRICATION OF SELF-ALIGNED SHORT CHANNEL COUNTER-DOPED 4H-SIC DMOSFETS

7.1 Mask Layout

The DMOS test layout which has a die size of 17 mm x 17 mm is shown in Fig. 7.1. The basic grouping of the chip containing all the transistors and test structures is shown in Fig. 7.2. This chip was repeated so that all the similar sized devices can be grouped together within the die. The die was then repeated across the mask. The self-aligned short-channel DMOS process consists of 10 mask levels described as follows:

1. P-well Implant Mask – Light Field Liftoff Mask
2. Registration Mask – Dark Field Etch Mask
3. n^+ Source Implantation Block Mask – Dark Field Liftoff Mask
4. p^+ Contact Implantation Mask – Light Field Liftoff Mask
5. JTE Implantation Mask – Light Field Liftoff Mask
6. Gate Pattern Mask – Light Field Etch Mask
7. p^+ Contact Mask – Dark Field Liftoff Mask
8. n^+ Contact Mask – Dark Field Liftoff Mask
9. SOG Window Open Mask – Dark Field Etch Mask
10. Top Metal – Dark Field Liftoff Mask

The masks were designed using Mentor Graphics IC Station and fabricated by Photronics Inc. [53]. Each chip can be described as follows:

1. One 3 mm x 3 mm device with JFET length of 6 μm (device 10 in Fig. 7.2)
2. Four 1.5 mm x 1.5 mm devices with JFET length of 6 μm (devices 11 through 14 in Fig. 7.2)

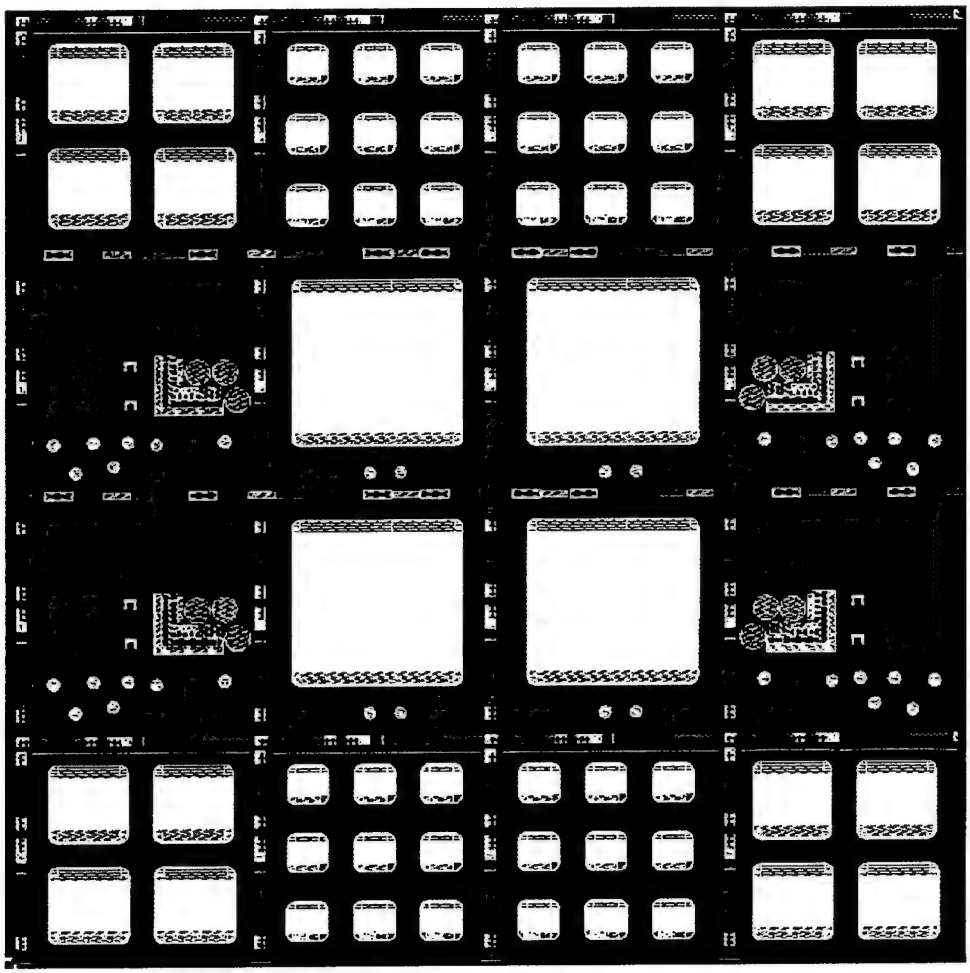


Fig. 7.1. A 17 mm x 17 mm DMOS die layout.

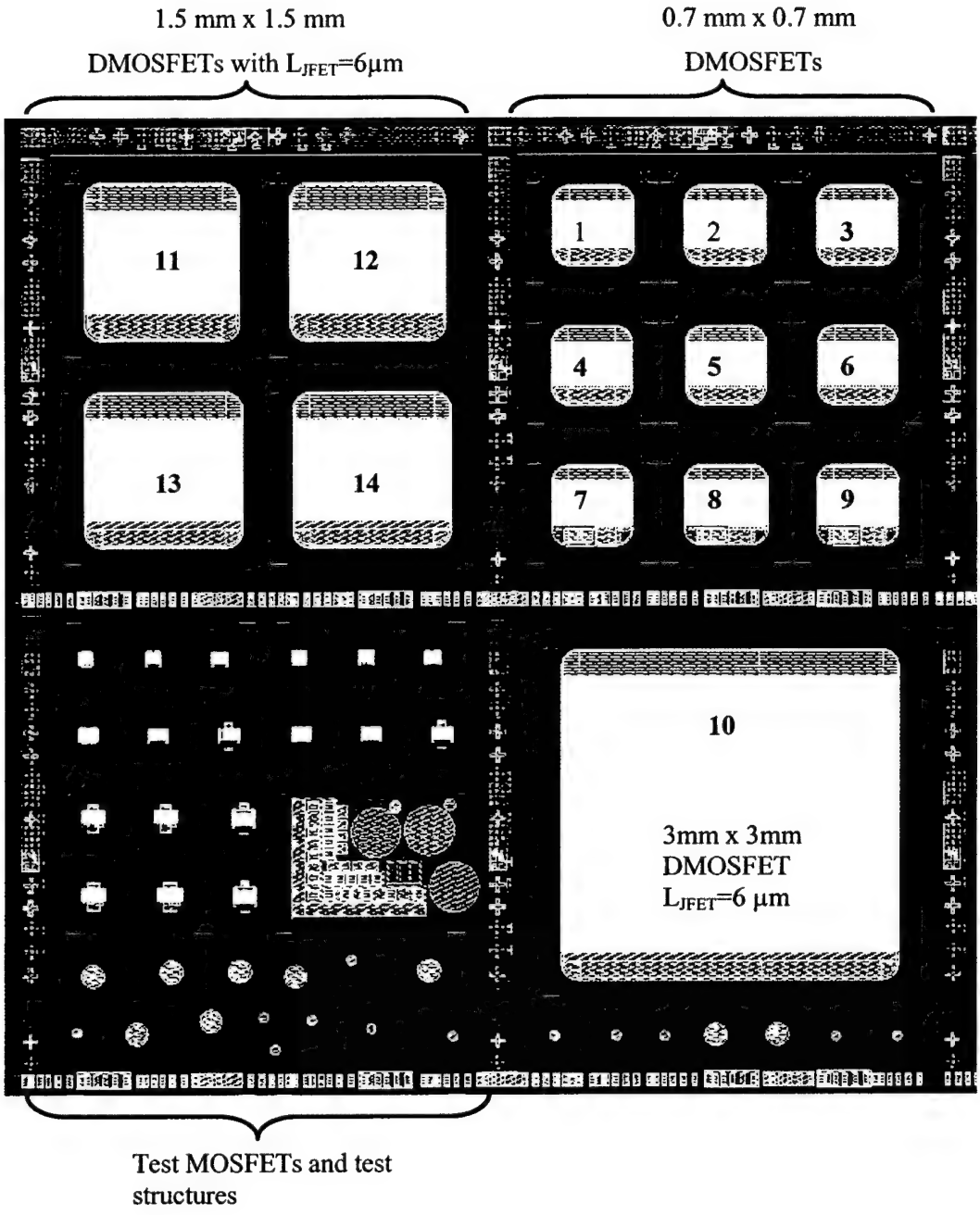


Fig. 7.2 An 8.5mm x 8.5mm chip containing all the devices and test structures.

3. Six 0.7 mm x 0.7 mm DMOS devices with JFET length of 6 μm (devices 1 through 6 in Fig. 7.2)
4. One 0.7 mm x 0.7 mm DMOS device with a JFET length of 3 μm (device 7 in Fig. 7.2).
5. One 0.7 mm x 0.7 mm DMOS device with a JFET length of 4 μm (device 8 in Fig. 7.2).
6. One 0.7 mm x 0.7 mm DMOS device with a JFET length of 5 μm (device 7 in Fig. 7.2).

The large area devices were designed to achieve higher on-currents. However, the yield of the large area devices will depend on defect density. With a reasonable current density of $J=100A/cm^2$ and defect density of $d_0=10/cm^2$, the yield of a 3 mm x 3 mm device [yield $=\exp(-d_0A)$] is 40% and the current rating is 9A. In a real device, the defect density can be from 15 to 30 $/cm^2$ and the large area devices will be limited by these defects. In the small test DMOSFET structures, the JFET length is 4, 6 and 8 μm. All the large and small DMOS structures have a self-aligned channel length of 0.5 μm. A JTE (Junction Termination Extension) was used for all DMOS structures.

P^+- n^- -n^+ diodes were drawn to monitor the p^+-n^- breakdown strength. Diodes with different JTE widths were laid out in order to check the JTE effect on breakdown voltage. MOS capacitors on n- drift region, on p-channel with the retrograde profile, and on n^+ source region were drawn to check the oxide quality and oxidation rates in these regions. Lateral MOSFETs with channel length of 3, 5, 10 and 20 μm were drawn. FATFETs with channel length of 50, 80, 110 and 140 μm were laid out to determine the inversion channel mobility. All lateral FETs were isolated by a p^+ implant.

7.2 Self-Aligned Short-Channel Counter-Doped DMOS Fabrication Process

7.2.1 Wafer specifications

Two 4H-SiC wafers were processed to fabricate the self-aligned short-channel counter-doped DMOS transistors. The first wafer is a heavily doped ($6.1 \cdot 10^{18}$ cm^{-3}) 35 mm diameter n^+ substrate with a 50 μm thick and $9 \cdot 10^{14}$ cm^{-3} lightly doped n^- drift layer, and the second wafer is a 20 mΩ-cm heavily doped 50 mm diameter n^+ substrate with a 20 μm thick and $3.2 \cdot 10^{15}$ cm^{-3} doped n^- drift layer as received from Cree Inc. Once the wafers were cleaned, a $400A^0$ sacrificial SiO_2 layer was grown by thermal oxidation. Figure 7.3 shows the device cross-section at this point.

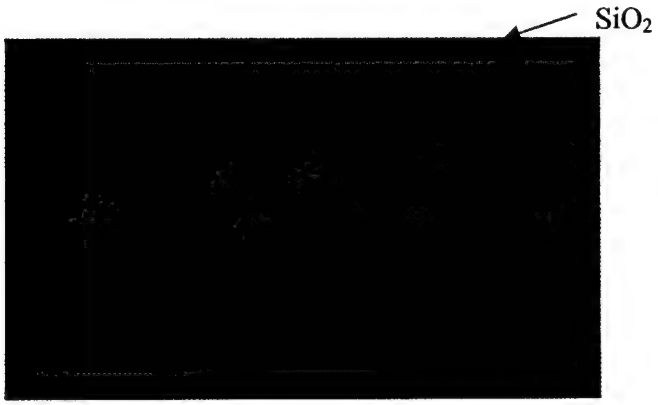
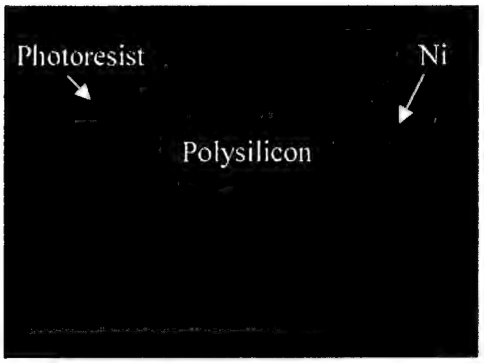


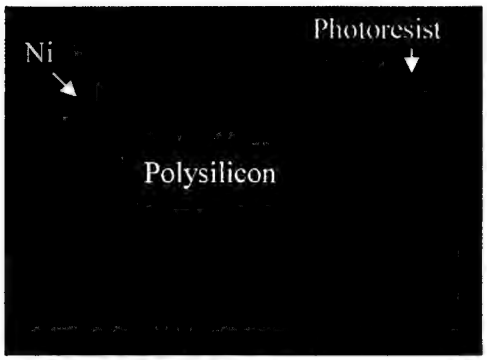
Fig. 7.3. Initial wafer cross-section.

7.2.2 P-well implantation mask

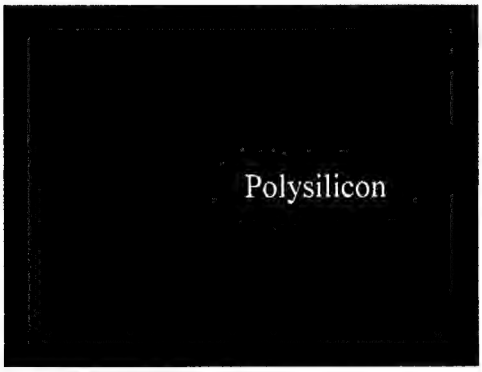
A 1.5 μm thick polysilicon layer was deposited by LPCVD at 600^0C with a SiH_4 flow rate of 50 sccm and 172 mTorr pressure. In order to get a uniform polysilicon deposition, two 2" silicon wafers were placed in front and two in back of the SiC wafers. A thin sacrificial SiO_2 layer was grown by oxidizing the polysilicon in wet O_2 at 900^0C for 10 minutes. The resulting oxide thickness is less than $350A^0$. The deposited polysilicon layer was then patterened by a $1900A^0$ thick Ti/Ni p-well mask-1 transferred by liftoff lithography. The polysilicon was patterened by RIE at 100W power, in SF_6 gas with a flow rate of 10sccm and a DC bias of 390 to 400V. To avoid any micro-masking at this high DC bias value, the nickel mask was covered with a thick AZ4620 photoresist layer (~6 μm thick), patterned with a different mask, which has features (~10 μm) larger than the p-well implant mask without the fingers. The RIE etch process was not uniform over the wafer, and alpha-step measurements showed a higher etch rate at the edge of the wafers. Figure 7.4 shows photographs of the 4H-50 μm 35 mm wafer at different etch steps. The RIE etch was performed in several steps to prevent any over etching of SiC material. The etch rate of polysilicon in SF_6 at 100W power was ~$900A^0$/min. The etch rate of AZ4620 positive photoresist was ~$880A^0$/min. Figure 7.5 shows SEM photographs of the polysilicon sidewall on the 4H-50 μm SiC sample after RIE.



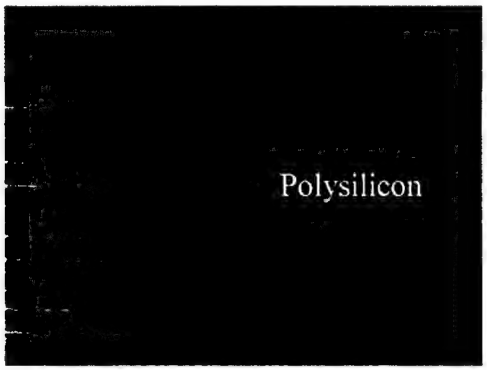
a) Before RIE etch of polysilicon.



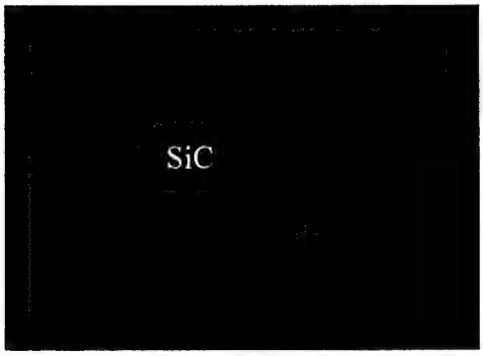
b) After 14 min RIE, wafer center.



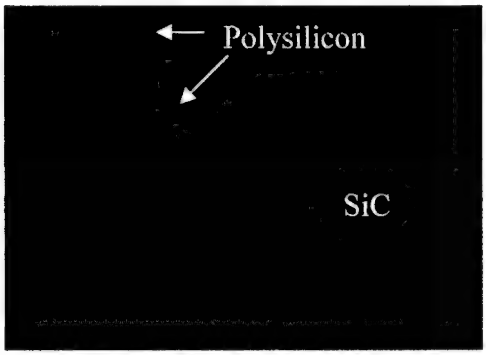
c) After 17 min RIE, wafer center.



d) After 17 min RIE, wafer edge.



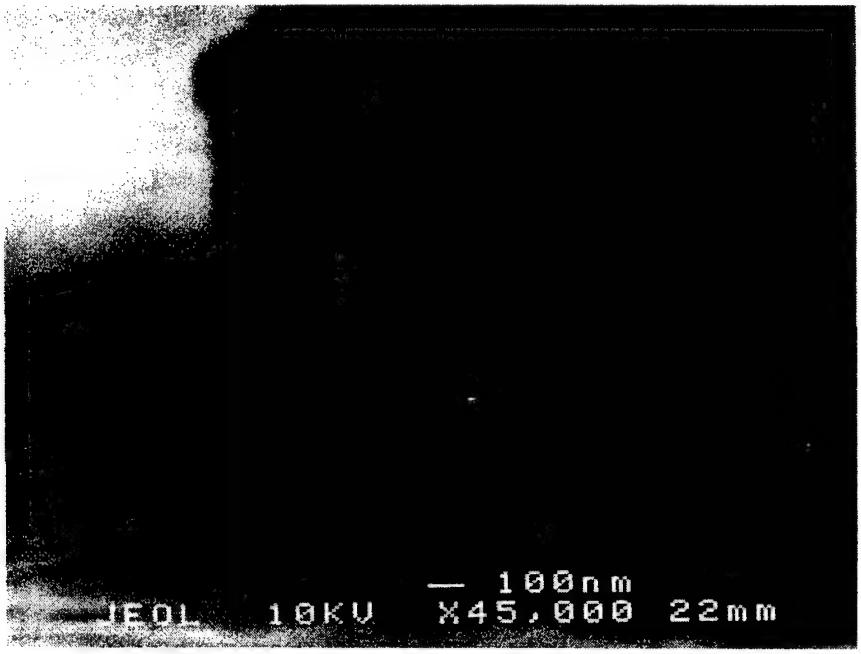
e) After 19 min RIE.



f) After photoresist and Ni mask removal.

Fig. 7.4. RIE etch of polysilicon mask at 100W power, in SF_6 gas at 10sccm and 400V DC bias. All photographs are taken under bright field and x500 magnification. Notice the difference in etch rate from wafer center to edge.

a) SEM photograph of the fingers after RIE etch.



b) SEM photograph of the polysilicon sidewall profile etched at 100W power, SF_6 gas and at 400V DC bias.

Fig. 7.5. SEM photographs of the polysilicon mask

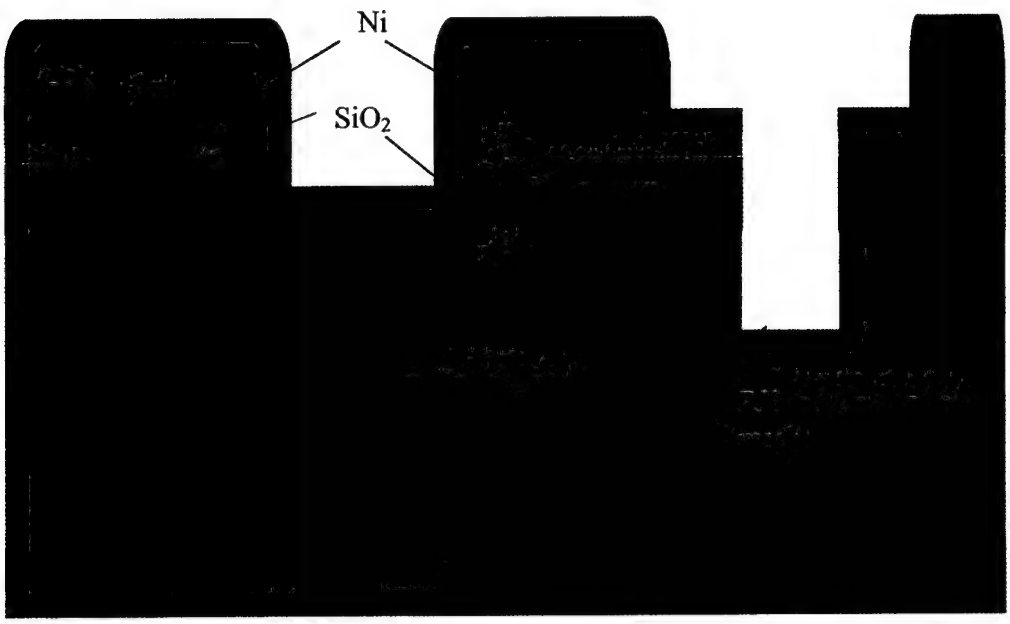


Fig. 7.6. Wafer cross-section after the registration etch.

After the RIE etch of the polysilicon layer, the AZ4620 photoresist was removed and again AZ4620 photoresist registration mask-2 was used to transfer registration marks on the wafers by RIE of SiC. The registration marks are self-aligned with the p-well implantation, which saves us 1μm of alignment tolerance. Figure 7.6 shows the wafer cross-section at this point.

7.2.3 P-well implantation profile

The p-type base region in power DMOS structures can be formed by ion implantation of boron (B) or aluminum (Al) into 4H-SiC material. Due to very small diffusion coefficients of these impurities, ion implantation is the only practical way to selectively dope SiC. However, to activate the dopants, anneal temperatures up to 1600-1700^{0}C are required to alleviate the lattice damage.

The p-type boron or aluminum serve as acceptors in SiC and substitute on the Si-lattice sites. Nitrogen or phosphorus serve as donors in SiC and substitute on C-lattice

sites. B atoms are lighter than Al atoms and therefore can be implanted deeper into SiC for a given implantation energy. For this reason, the implantation damage introduced by Al is also more severe than B. Ramungul et al. [54] have investigated Al and B implanted p^+-n junctions in 6H-SiC and found B implanted diodes exhibit an order of magnitude lowered leakage currents than the Al diodes, as B causes less implantation damage. Typical ionization energies for acceptors in 4H-SiC material is given below [55].

$$\Delta E_A(\text{Al-shallow}) = 191 \text{ to } 230 \text{ meV}$$
$$\Delta E_A(\text{B-shallow}) = 285 \text{ to } 390 \text{ meV}$$
$$\Delta E_A(\text{B-deep}) = 540 \text{ to } 720 \text{ meV}$$

The reason for two ionization energies is that, in 4H-SiC there are two Si-sites, one with cubic surrounding and the other with hexagonal surrounding [55]. B atoms substituting on these sites experience different surroundings and give rise to different ionization energies. For Al-doped 4H-SiC, only one energy level is considered as the energy difference between the two different energy levels corresponding to the two lattice sites, is too small to detect [56]. Al has a lower activation energy compared to B, and therefore has less carrier-freeze-out at room temperature and yields higher hole concentrations. The Al diodes, investigated by Ramungul [54], showed x200 smaller on-resistances compared to the B implanted diodes.

B has the largest diffusion coefficient at an elevated temperature. Troffer et al. [56] investigated the annealing behavior of high dose Al and B implants into 4H-SiC, where SIMS profiles show broadening of the implanted B profile after a 1700^0C anneal step in a SiC crucible for 30 minutes. Both Al and B implants showed a diffusion tail. However, the B implanted sample showed a larger diffusion tail, and significant out-diffusion of B occurred which resulted in a pile-up of the B concentration near the SiC surface. This vertical diffusion nature of the B implants into the channel region of a DMOS structure can affect the electrical characteristics by changing the counter-doped or accumulation layer from n-type to p-type.

Saks et al. [57] investigated activation of low dosed Al and B implants in 4H-SiC material. After a 1600^0C anneal in a Si-overpressure ambient, aluminum implants showed 77% activation while the boron activation was only 22%. SIMS profiles show significant out-diffusion of boron near the surface due to evaporation of boron after the high temperature anneal step, and also showed a long diffusion tail of 1 μm beyond the maximum implantation depth. Although the B implanted sample showed a slightly higher bulk mobility value, the activation anneal temperature of Al was much lower, and a more uniform implantation profile was obtained.

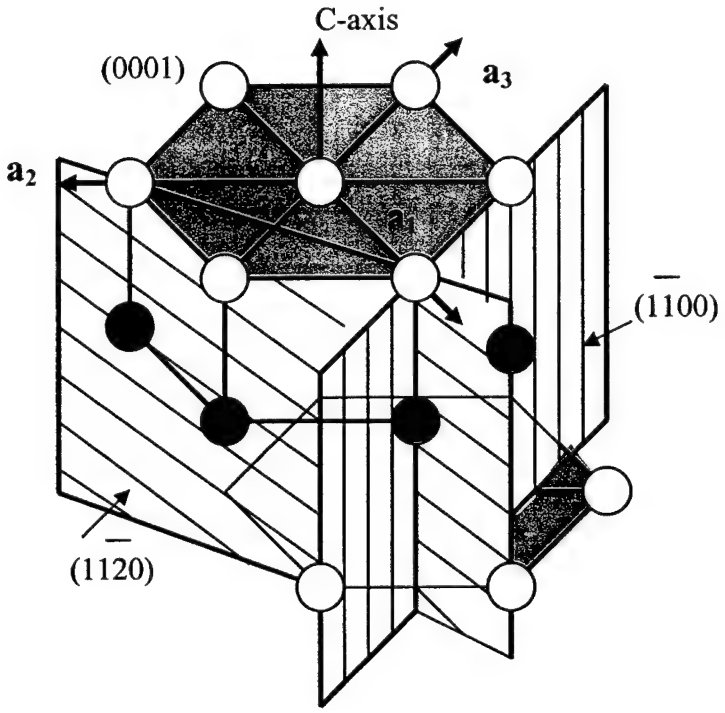


Fig. 7.7. A-faces of SiC MOSFETs.

Kumar et al. [58] investigated the vertical and lateral diffusion of B into 4H-SiC material. For this purpose a single step high energy B implantation was performed on (0001), $(1\bar{1}00)$ and $(11\bar{2}0)$ oriented 4H-SiC wafers (Fig. 7.7 shows the a-faces), where the (0001) oriented wafer represented the vertical diffusion and the a-face oriented wafers

represented the lateral diffusion of B on a SiC power DMOS structure. After annealing the samples at 1600^0C for 30 minutes in argon, the resulting SIMS profile showed significant lateral diffusion (a-face) of the B implants compared to the vertical diffusion, as shown in Fig. 7.8. For a short channel DMOS structure, B induced lateral diffusion can result in increasing of the channel length and decreasing of the adjacent p-well spacing. In order to achieve low specific on-resistances in SiC power MOSFETs, we need a high channel density and a smaller cell pitch. In the DMOS structure, the cell pitch is limited by the channel length and JFET length. As the channel length is increased and the JFET gap is decreased, the specific on-resistance can therefore increase considerably. In order to ensure short channel length, $L_{ch} \leq 0.5\mu m$ in this experiment, the p-wells are formed by implanting Al into 4H-SiC material.

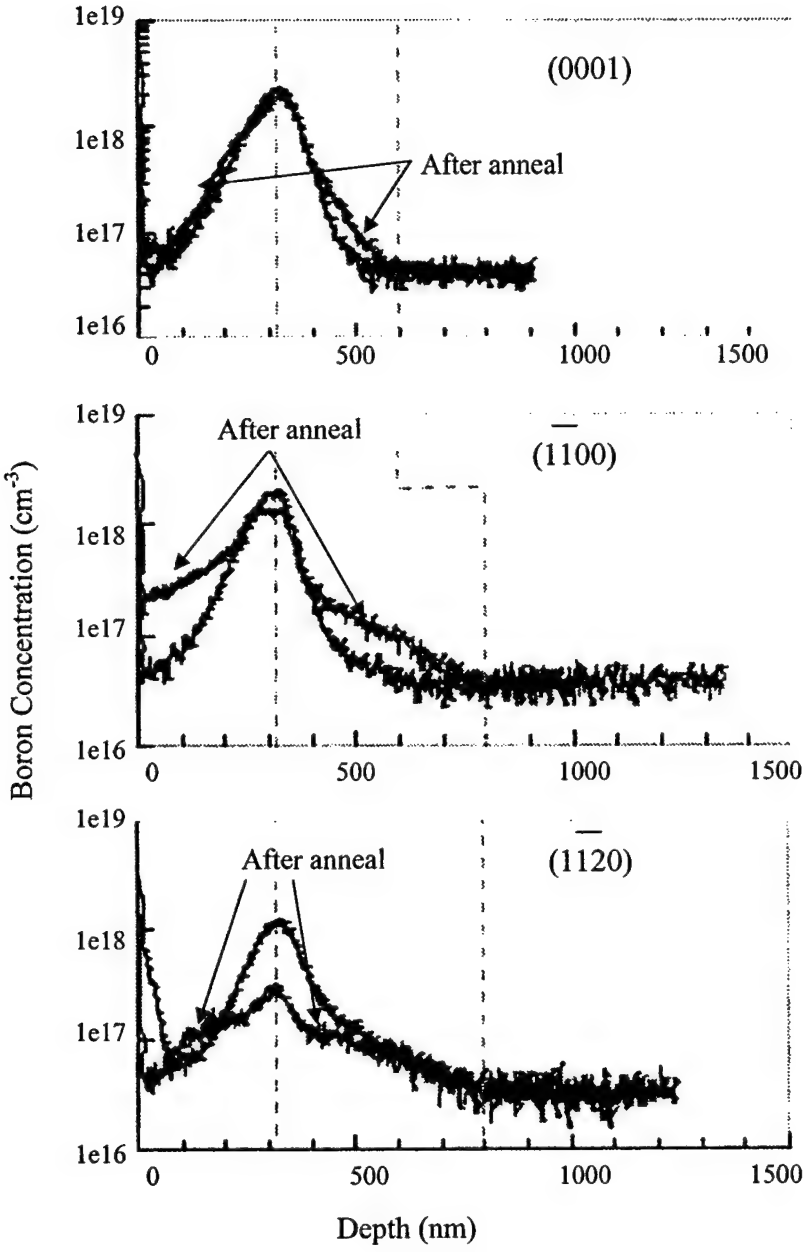


Fig. 7.8. SIMS profile of B induced lateral and vertical diffusion into a 4H-SiC sample after a 1600^{0}C, 30 minute anneal. The B diffusion is more pronounced in the a-faces compared to the c-face[58].

Table 7.1 shows the dose and energy used to form the retrograde p-well by implanting Al. The channel p-type doping concentration is around $5 \cdot 10^{17}$ cm^{-3} and the bottom p^+ implant concentration is near $3 \cdot 10^{18}$ cm^{-3}.

Table 7.1

Implant Species	Aluminum
Temperature	650^0C
Total Dose (cm^{-2})	$8.9 \cdot 10^{13}$
Energy (keV)	Dose (cm^{-2})
60	$1.6 \cdot 10^{12}$
100	$2.4 \cdot 10^{12}$
260	$2.2 \cdot 10^{12}$
360	$6.3 \cdot 10^{12}$

The counter doping is performed with a single energy step and the schedule is shown in Table 7.2. In order to prevent any n-type counter-dopants to go into the JFET region under the gate, the counter-doping is introduced at the same time as the p-well implantation and thus remains in the channel region. Figure 7.9 shows the implantation profiles obtained from TRIM simulations.

Table 7.2

Implant Species	Nitrogen
Temperature	650^0C
Total Dose (cm^{-2})	$3.4 \cdot 10^{12}$
Energy (keV)	Dose (cm^{-2})
30	$3.4 \cdot 10^{12}$

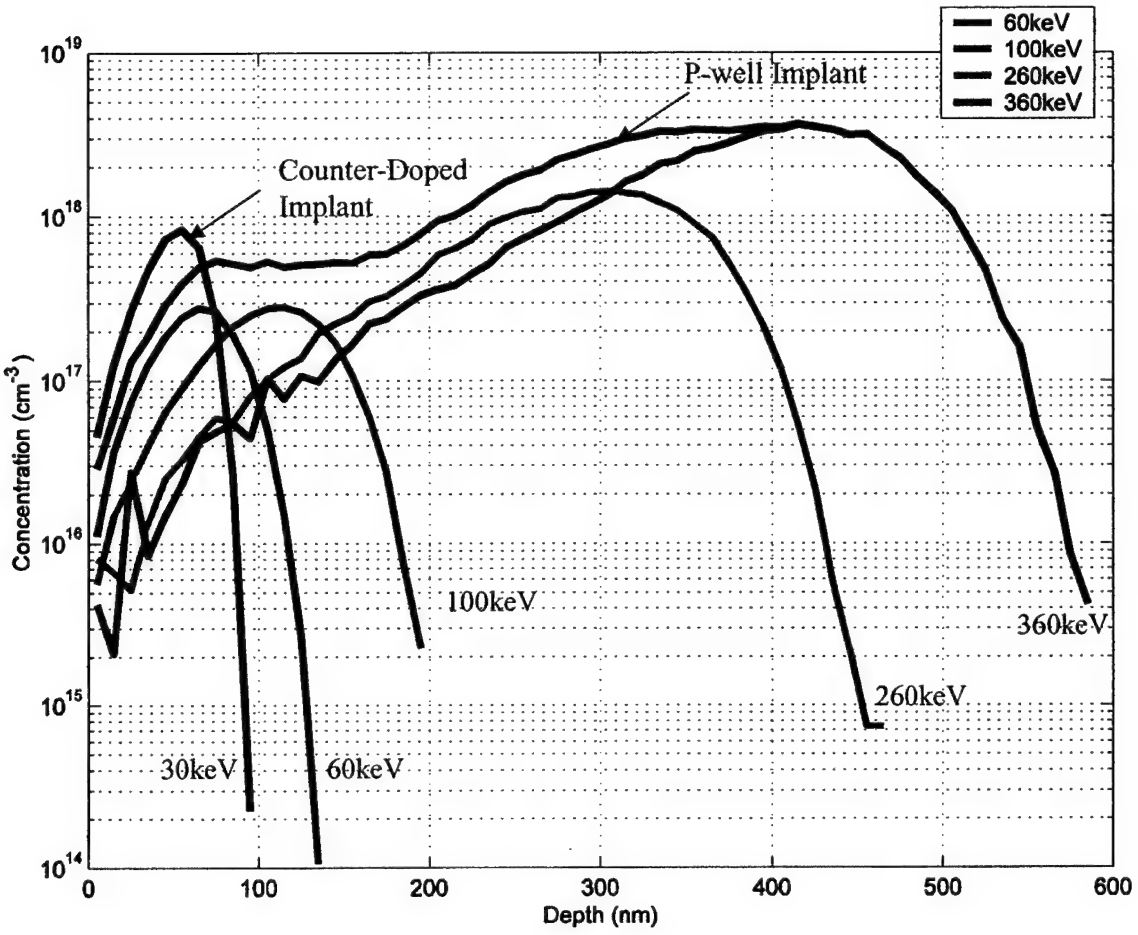


Fig. 7.9. P-well retrograde implant and n-type counter-doped implant.

The counter-doped implant is designed such that the implantation depth is ~85nm. Assuming 25nm are oxidized during the gate oxidation process, this leaves only 60nm of n-type implantation with a peak concentration of $8 \cdot 10^{17}$ cm^{-3}. Assuming 100% activation of the counter-doped and the p-type channel implants, after compensation the counter-doped dose becomes $(N_D-N_A)X_N=(8 \cdot 10^{17}\ cm^{-3} - 5 \cdot 10^{17}\ cm^{-3}\ )60nm=1.8 \cdot 10^{12}\ cm^{-2}$. If we assume 50% activation of the p-channel implant, the counter-doped dose is $(8 \cdot 10^{17}\ cm^{-3} - 2.5 \cdot 10^{17}\ cm^{-3})60\ nm=3.3 \cdot 10^{12}\ cm^{-2}$. During the polysilicon oxidation process, if we assume an additional 10nm of the N_D implant is removed, then the counter-doped dose

assume an additional 10nm of the N_D implant is removed, then the counter-doped dose after compensation and activation is about ($3.4 \cdot 10^{12}$ cm^{-2} -$2.5 \cdot 10^{17}$ cm^{-3}x50 nm) = $2 \cdot 10^{12}$ cm^{-2}, and with 100% activation of the p-type channel implants, the counter-doped dose is about ($3.4 \cdot 10^{12}$ cm^{-2}- $5 \cdot 10^{17}$ cm^{-3}x50 nm) $\approx 1 \cdot 10^{12}$ cm^{-2}. It is very difficult to design the counter-doped implant dose to get a high channel mobility value and at the same time maintain a normally off condition as the activation % of the Al is not known very accurately. Figure. 7.10 shows the wafer cross-section at this point.

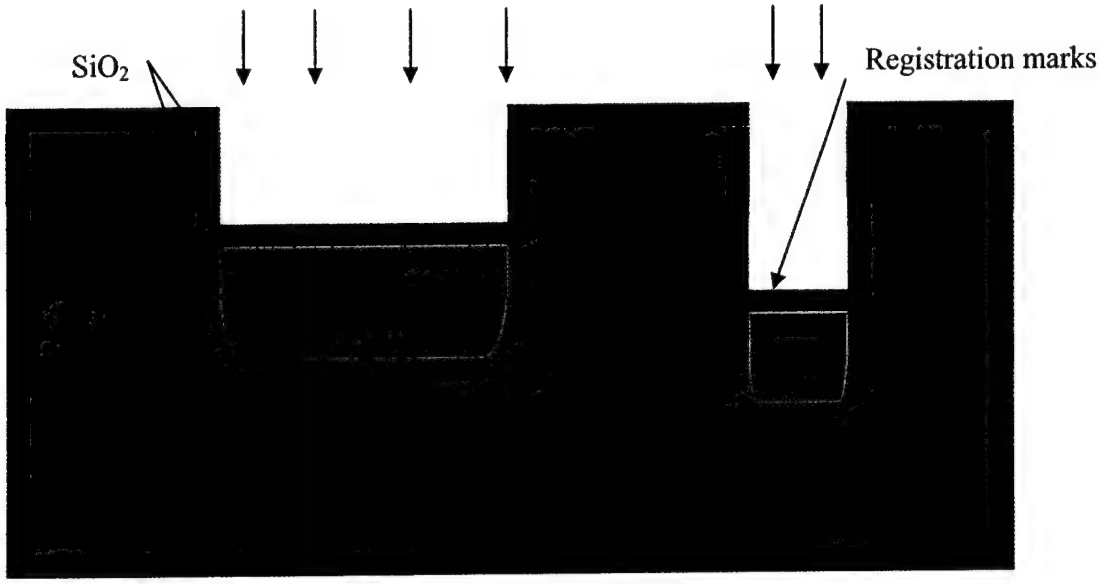


Fig. 7.10. Wafer cross-section after the p-well and counter–doped implantations.

7.2.4 Self-aligned source process

After the p-well and counter-doped implantation, the polysilicon thickness was measured by alpha-step. SEM photographs of the alignment marks were also taken before the oxidation step. From previous experiments described in section 6.3 we have seen two

different oxide thicknesses on the patterned polysilicon fingers. The oxide thickness on the sidewall of the polysilicon finger is smaller than the one on the top surface. A channel length of 0.5 μm was obtained with t_{ox}=1.2 μm on the top surface. To monitor the polysilicon oxide thickness, two SiC test pieces were also used. After cleaning the wafers and test pieces, all were oxidized at 1000^0C in wet O_2 for 6hrs. The resulting oxide thickness calculated on one of the test pieces (6H-SiC) was t_{ox}= [2.1 μm (after oxidation)-1.5 μm (original poly)]/0.54 =1.1 μm, which is less than the target oxide thickness of t_{ox}=1.2 μm. The wafers were then re-oxidized for an additional 3hrs. The resulting (poly-oxide plus unoxidized poly) thickness was found to be 2.3 μm and the calculated oxide thickness was t_{ox}=(2.3-1.53)/0.54=1.43 μm after the 9 hr oxidation (see Fig. 7.11). A thin layer ($35A^0$) of Au was then deposited on the test pieces and the 4H-50μm wafer by e-beam evaporation. SEM photographs of the alignment marks were re-taken after the oxidation process. Due to the two different oxide thicknesses over an etched polysilicon pattern, although the polysilicon in the vertical direction showed a larger oxide thickness, the channel length obtained from the SEM measurements on the 4H-50 μm sample was ~ 0.38 to 0.42 μm (after 9 hrs of oxidation). Figure 7.12 summarizes the self-aligned source experiments and channel length determination on the 4H-50 μm wafer.

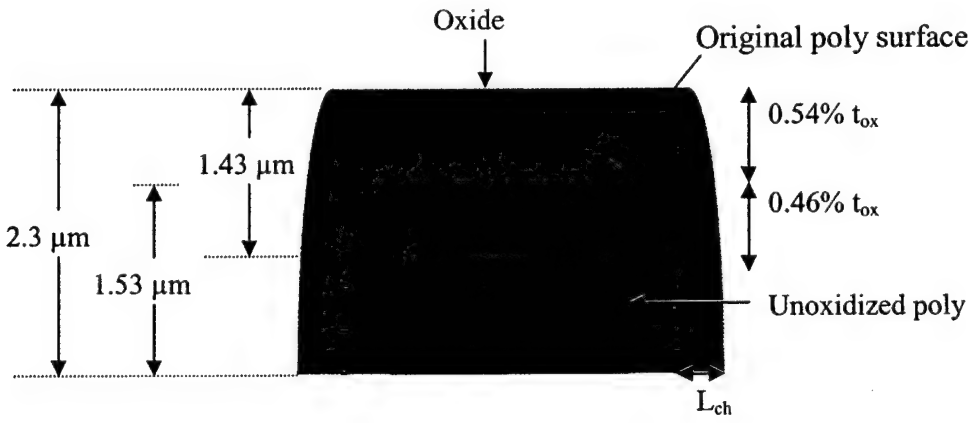
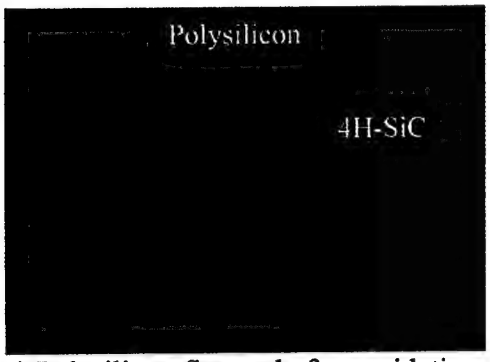
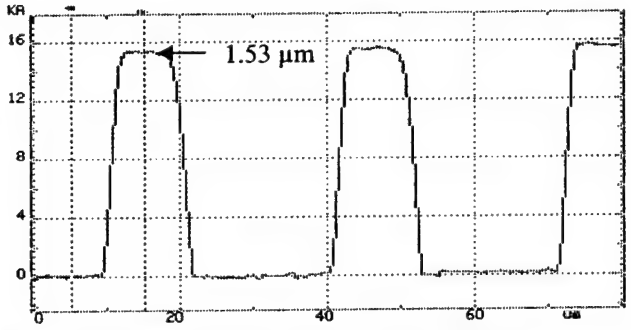


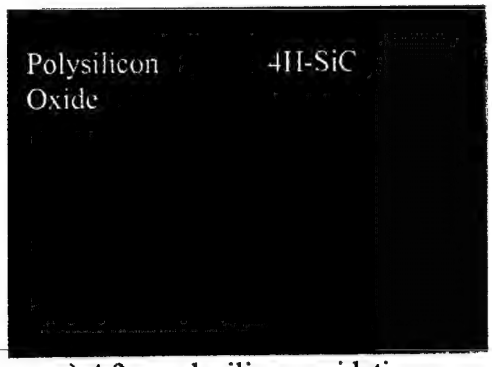
Fig. 7.11. Oxide thickness calculation after the 9 hr poly oxidation.



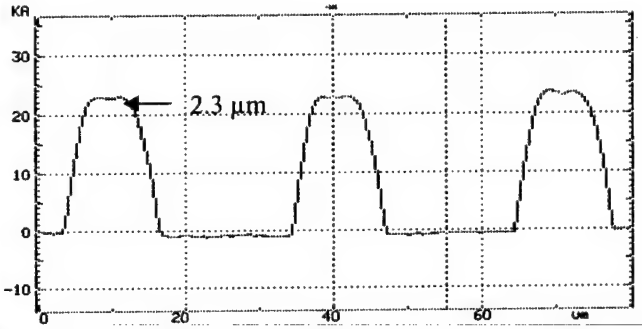
a) Polysilicon fingers before oxidation magnification x500.



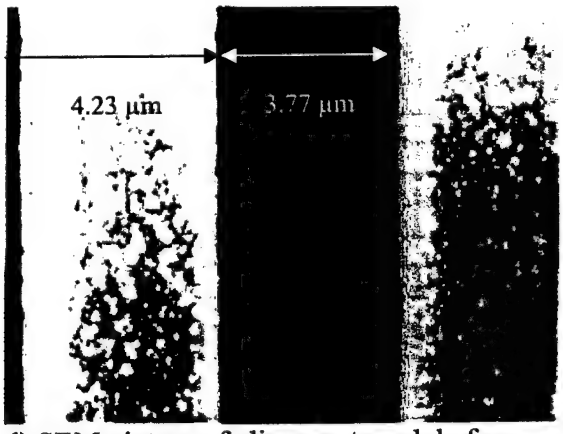
b) Alpha step measurement of the fingers of a 3 mmx3 mm device on the 4H-50µm wafer before oxidation.



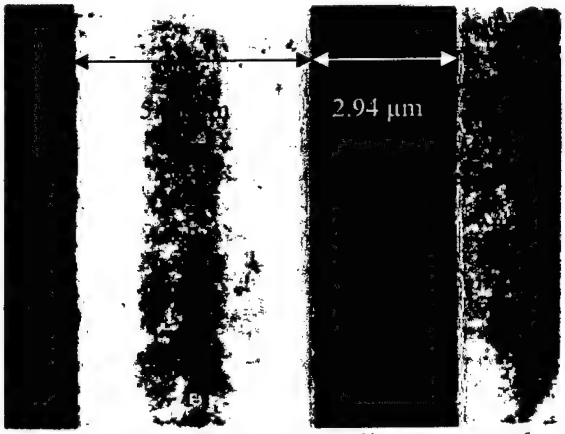
c) After polysilicon oxidation magnification x500.



c) Alpha step measurements after the 9hr oxidation.



d) SEM picture of alignment mark before oxidation on 4H-50µm wafer.



e) SEM picture of the same alignment mark after oxidation.

Fig. 7.12. Self-aligned source experiments on the 4H-SiC 50 µm wafer. The resulting channel length varied from 0.38 µm to 0.42 µm.

In order to monitor the oxidation rates of the un-annealed p-well and counter-doped implantations, a small 4H-SiC test piece with the same p-well and counter-doped implantation as the real SiC wafers, was oxidized at the same time. The oxide thickness measured after the 9 hr polysilicon oxidation was less than $250A^0$.

7.2.5 N^+ source implantation

In order to block the source implantation on some areas where later a p^+ contact implantation is performed, a Ti/Au ($100/4000A^0$) layer is deposited and patterned by liftoff lithography. The n^+ source implantation is then performed by implanting nitrogen with the implantation dose and energy schedules given in Table 7.3.

Table 7.3

Implant Species	Nitrogen
Temperature	650^0C
Total Dose (cm^{-2})	$3.3 \cdot 10^{15}$
Energy (keV)	Dose (cm^{-2})
30	$7.0 \cdot 10^{14}$
70	$1.0 \cdot 10^{15}$
120	$1.6 \cdot 10^{15}$

Figure 7.13 shows the source implantation profile with a peak concentration of $1 \cdot 10^{20} cm^{-3}$ and a junction depth of 0.25 μm. Figures 7.14a and b show the wafer photograph and device cross section at this point.

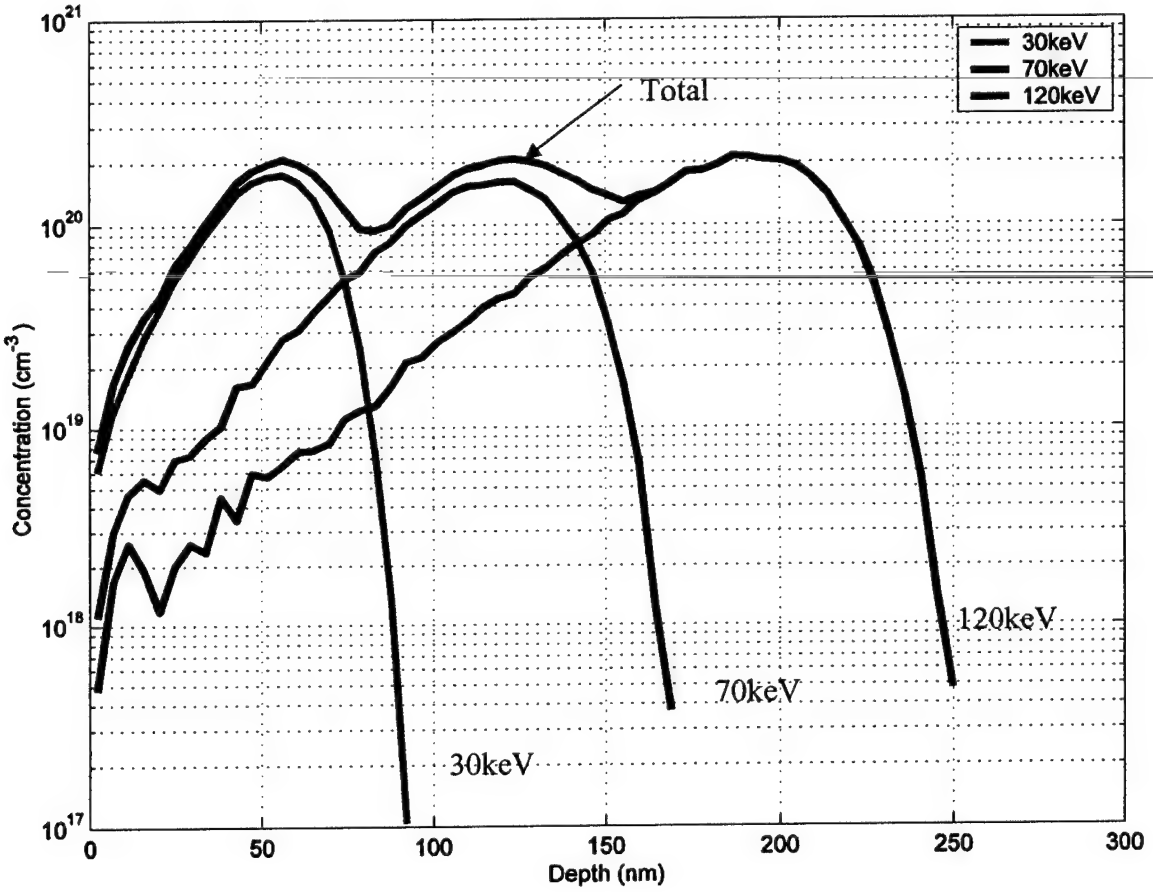
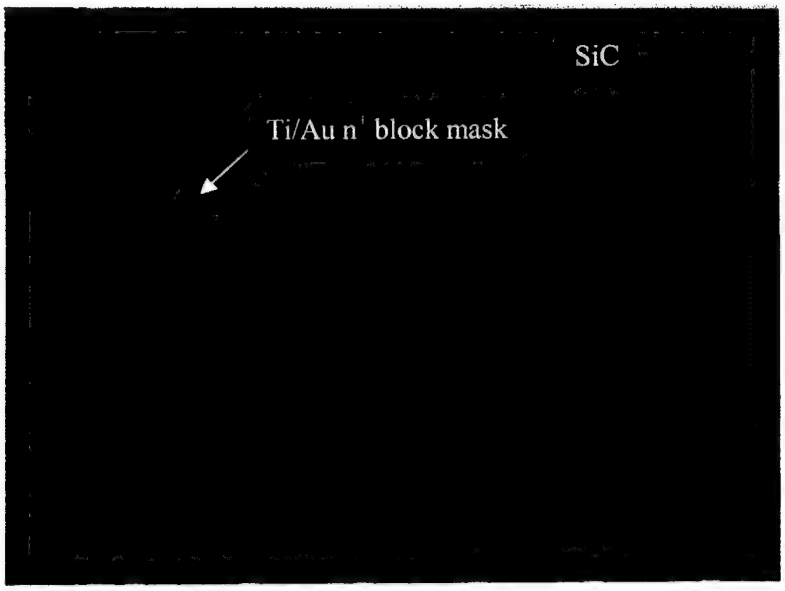
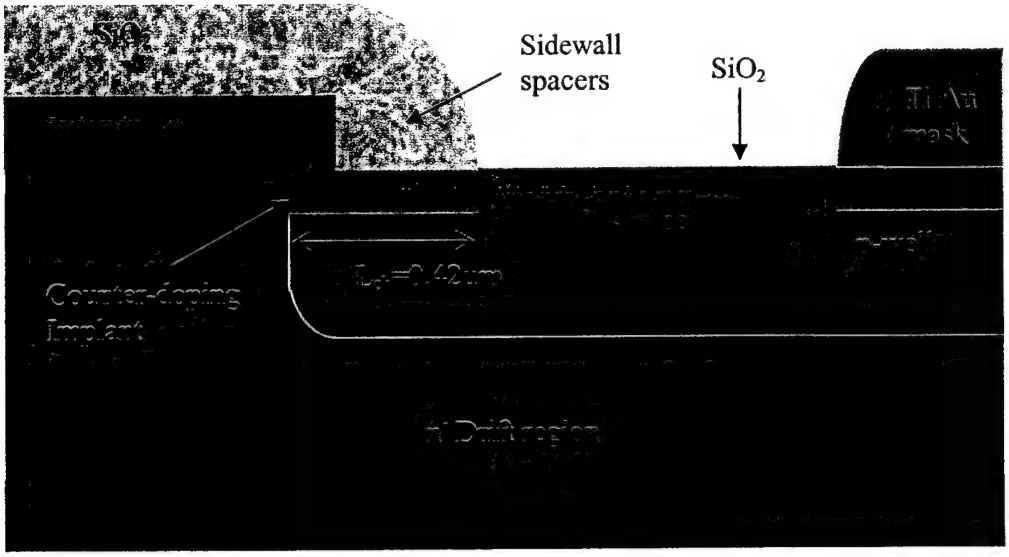


Fig. 7.13. N^+ source implantation profile.



a) Ti/Au layer deposited by e-beam evaporation to block the n^+ source implantation. Photograph of 4H-20μm wafer after n^+ source implantations. Magnification x500.



b) Wafer cross-section after source implantation.

Fig. 7.14. Wafer photograph and cross-section after the source implantation.

7.2.6 P^+ contact implantation

After the n^+ source implantation, the metal mask, SiO_2 layer, and un-oxidized polysilicon layers were removed. A $200A^0$ SiO_2 layer was then re-deposited by e-beam evaporation in the Leybold evaporator. A $100/6000A^0$ of Ti/Au p^+-implant mask-4 was then transferred by liftoff lithography. A p^+ contact implantation was then performed by implanting aluminum into SiC. The implantation schedule is given in Table 7.4.

Table 7.4

Implant Species	Aluminum
Temperature	650^0C
Total Dose (cm^{-2})	$1.05 \cdot 10^{15}$
Energy (keV)	Dose (cm^{-2})
40	$1.0 \cdot 10^{14}$
100	$2.0 \cdot 10^{14}$
180	$2.5 \cdot 10^{14}$
280	$5.0 \cdot 10^{14}$

Figure 7.15 shows the p^+ contact implantation profile with a peak concentration of $3 \cdot 10^{18}$ cm^{-3} and implantation depth of 0.4μm. Figure 7.16a) shows the wafer photograph after the Ti/Au liftoff process, and b) the wafer cross-section after the p^+ contact implantation.

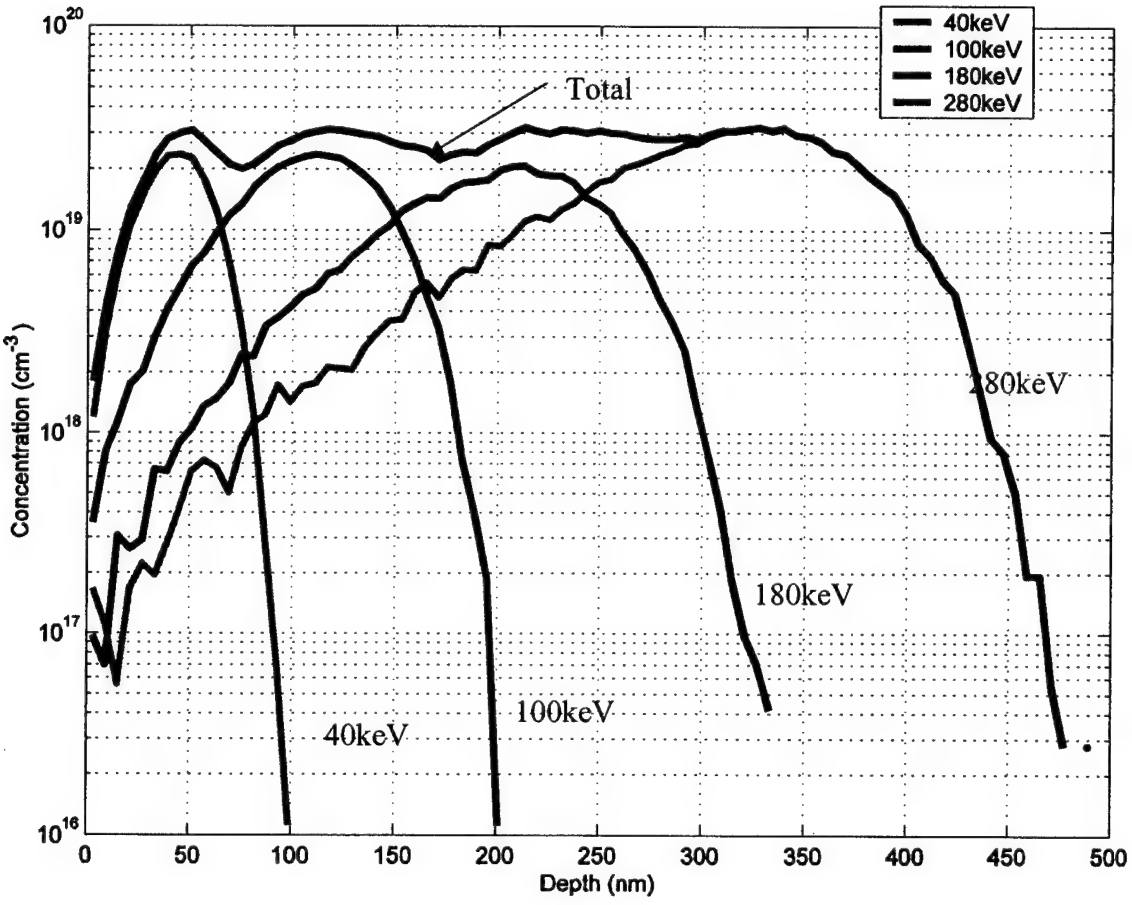
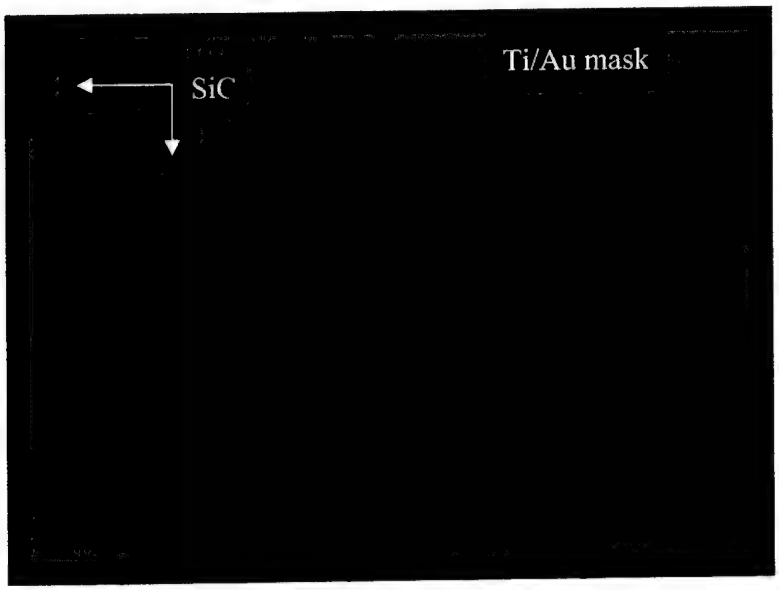
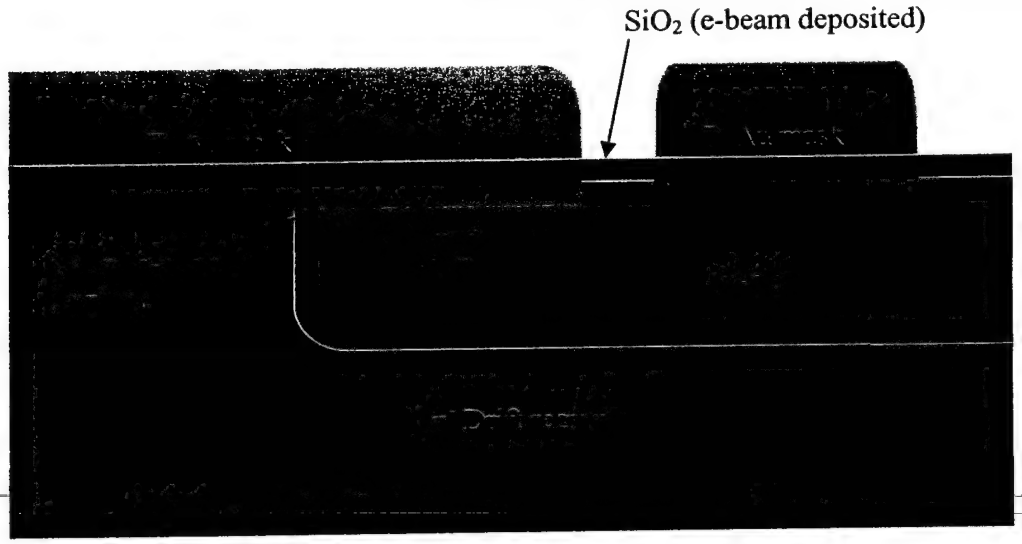


Fig. 7.15. P^+ contact implantation profile



a) Ti/Au layer deposited by e-beam evaporation. Wafer photograph of the 4H-20μm wafer after p^+ contact implantation. Magnification x500.



b) Wafer cross-section after p^+ contact implantation.

Fig. 7.16. Wafer photograph and cross-section after p^+ contact implantation.

7.2.7 JTE (Junction Termination Extension) Implantation

The optimum edge termination of the p^+ base and n^- drift junction is very critical in order to prevent premature junction breakdown due to electric field crowding at the device edge when a large reverse voltage is applied. For power SiC devices with drift region thickness less than 10 μm, a simple trench edge termination may be sufficient [11], but for drift layer thickness greater than 10 μm, an optimum edge termination ensures a breakdown voltage close to the ideal parallel plane value. In this process, the junction termination technique (JTE) [59] has been employed. This technique has been studied and experimentally verified on 4H-SiC UMOSFETs by Yu Li and Imran Khan [26],[27] of Purdue University.

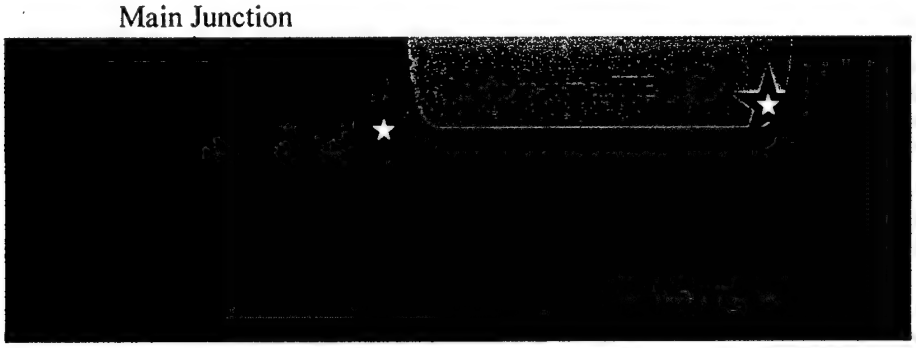


Fig. 7.17. Main junction with JTE edge termination.

Figure 7.17 illustrates the principle of the JTE technique, where a lightly doped p-layer is introduced by ion implantation near the main junction. The JTE is implanted to prevent electric field crowding at the edge of the main junction. The JTE dose is typically designed so that at the designed blocking voltage, the p-layer is fully depleted. For a critical electric field of $2 \cdot 10^6$ V/cm, the required JTE dose is then $Q = N_A X_{JTE} = \varepsilon_s E_{crit}/q = 1.1 \cdot 10^{13}$ cm^{-2}. If the JTE dose is too low, the JTE layer will deplete at a much lower voltage and the maximum electric field will be at the main junction, and consequently result in premature breakdown at the edge of the main junction. If the JTE dose

is too high, the JTE is not fully depleted, electric field crowding occurs at the JTE edge, and premature breakdown occurs at the JTE edge.

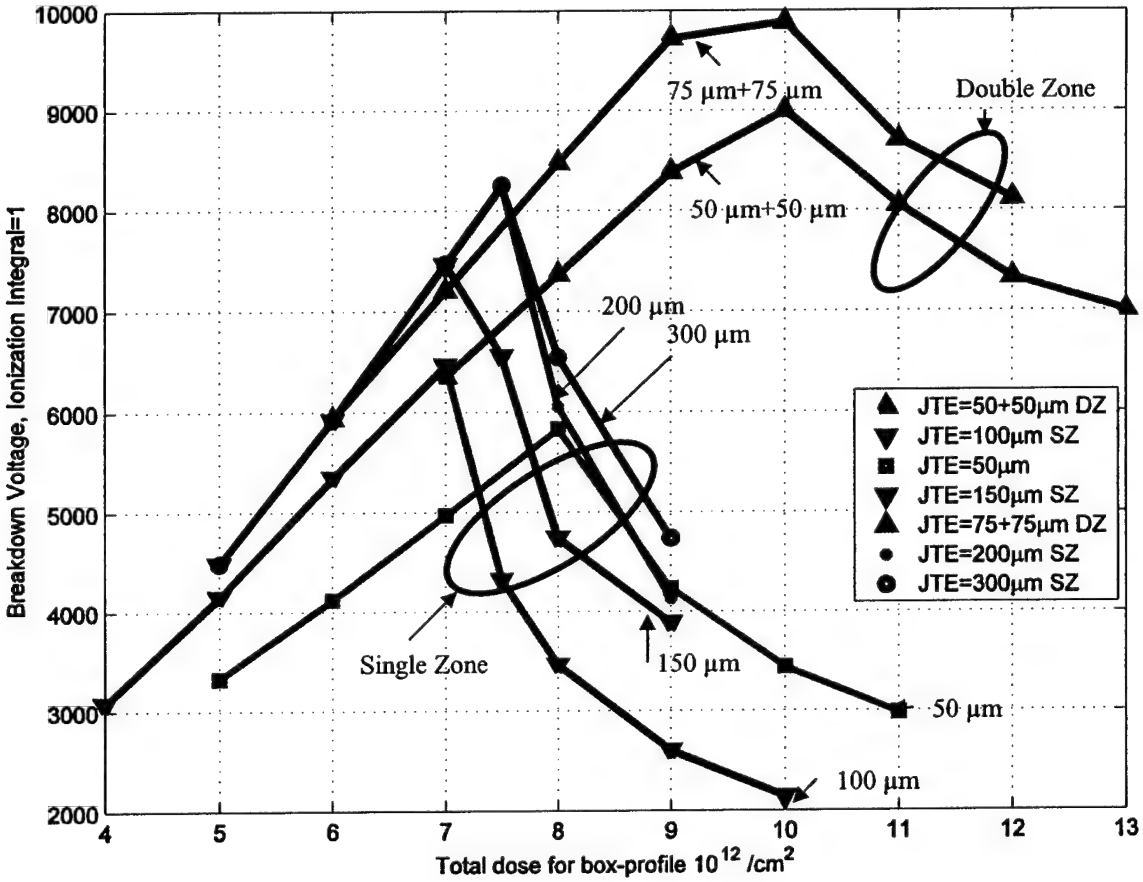


Fig. 7.18. Dependence of the breakdown voltage with variation in JTE dose and width [27]. Drift region thickness is 100 µm and doping is $6 \cdot 10^{14}$ cm^{-3}.

Figure 7.18 shows the effect of JTE dose and width, as obtained by MEDICI simulations [27]. The maximum breakdown voltage was determined when the ionization integral approached unity. Both single zone (SZ) and double zone (DZ) JTE structures were investigated for a UMOS structure with a drift region thickness of 100 µm and doping of $6 \cdot 10^{14}$ cm^{-3}. For SZ JTE structures, the sharp peaks in the breakdown voltage

thickness. The DZ JTE structures are simulated with the outer JTE dose fixed at $5.85 \cdot 10^{12}$ cm^{-2} (80% of the optimum dose for SZ JTE) and the inner JTE dose varied to get an optimum value. The DZ JTE structures are found to be less sensitive to the JTE dose and also more effective in protecting the main junction than the SZ structures. However, in the DZ structure, two different doses are required and thus require an extra photolithography and ion implantation step. In this process, a single zone JTE structure with a dose of $1.1 \cdot 10^{13}$ cm^{-2} (assuming 70% activation of the Al implants) and JTE width of 150 μm was formed by implanting aluminum into SiC. Table 7.5 shows the implantation schedule of the SZ JTE implant. Figure 7.19 shows the JTE implantation profile.

Table 7.5

Implant Species	Aluminum
Temperature	650^0C
Total Dose (cm^{-2})	$1.1 \cdot 10^{13}$
Energy (keV)	Dose (cm^{-2})
40	$1.0 \cdot 10^{12}$
100	$2.0 \cdot 10^{12}$
200	$3.0 \cdot 10^{12}$
350	$5.0 \cdot 10^{12}$

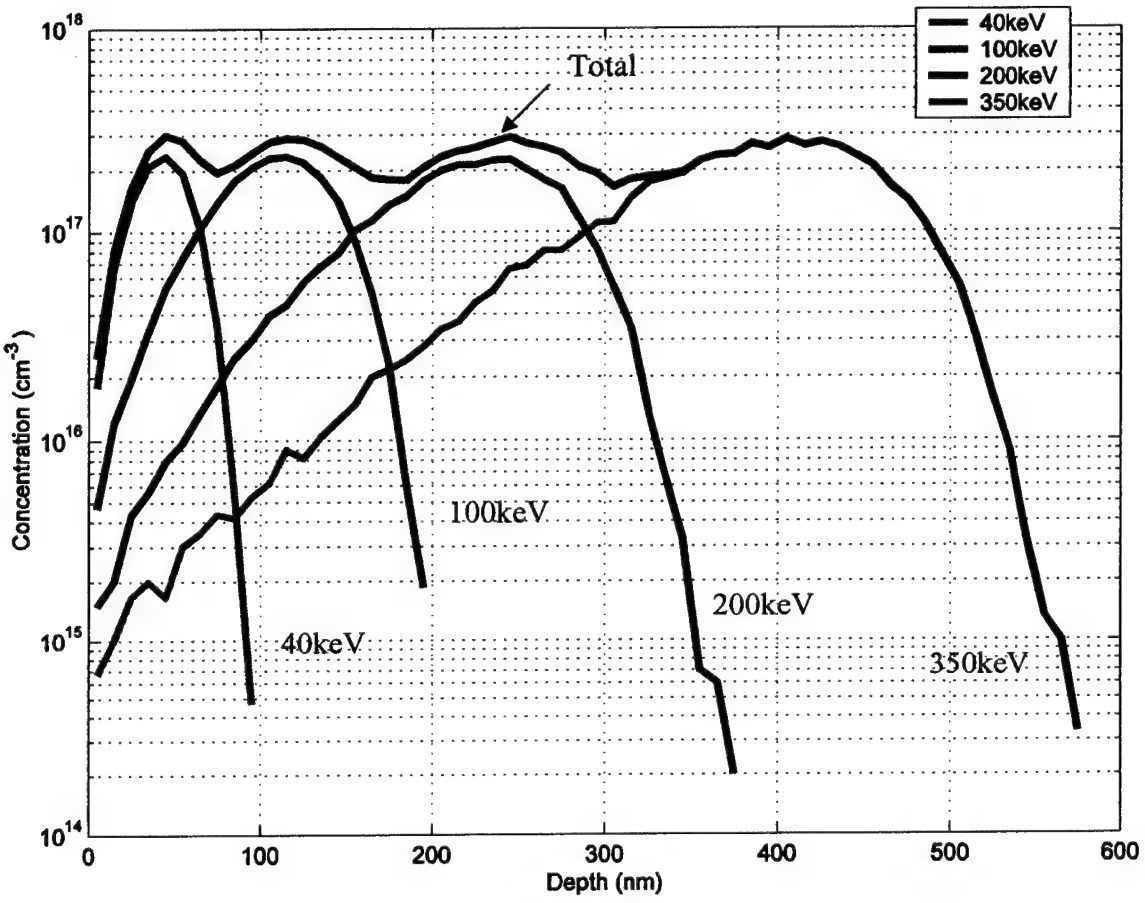
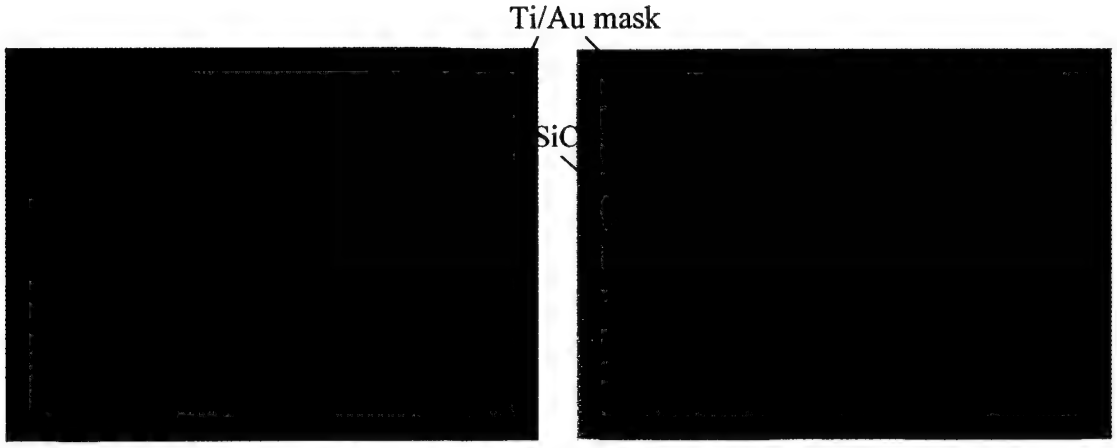


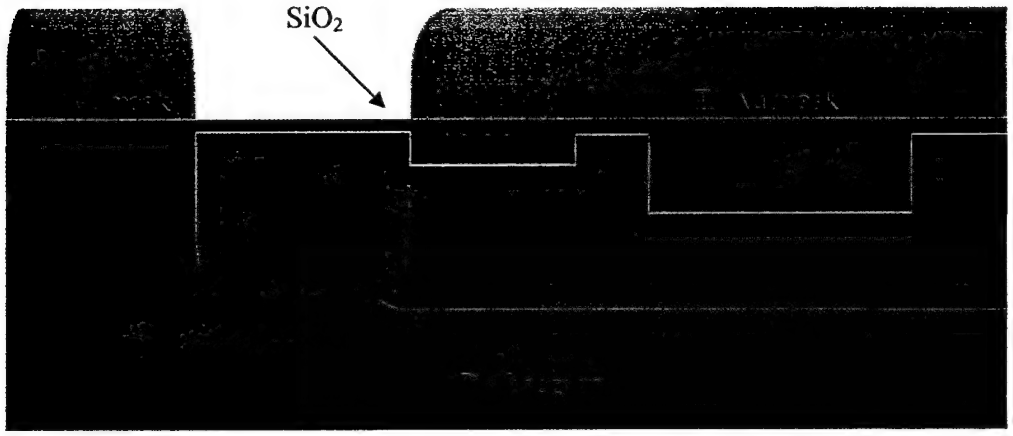
Fig. 7.19. Single zone JTE Implantation profile.

After the p^+ contact implantation, the metal mask and SiO_2 layer were removed. A $200A^0$ SiO_2 layer was then re-deposited by e-beam evaporation in the Leybold evaporator. $100/7000A^0$ of Ti/Au was e-beam evaporated and defined by liftoff lithography using JTE-implant mask-5. Figures 7.20a) and b) show wafer photographs after the JTE implantation step, and c) shows the cross-section of the wafers at this point.



a) 1.5mmx1.5mm device on the 4H-50μm wafer after Ti/Au mask deposition by e-beam evaporation. Magnification x50.

b) A small test DMOSFET on the 4H-50μm wafer magnification x200.

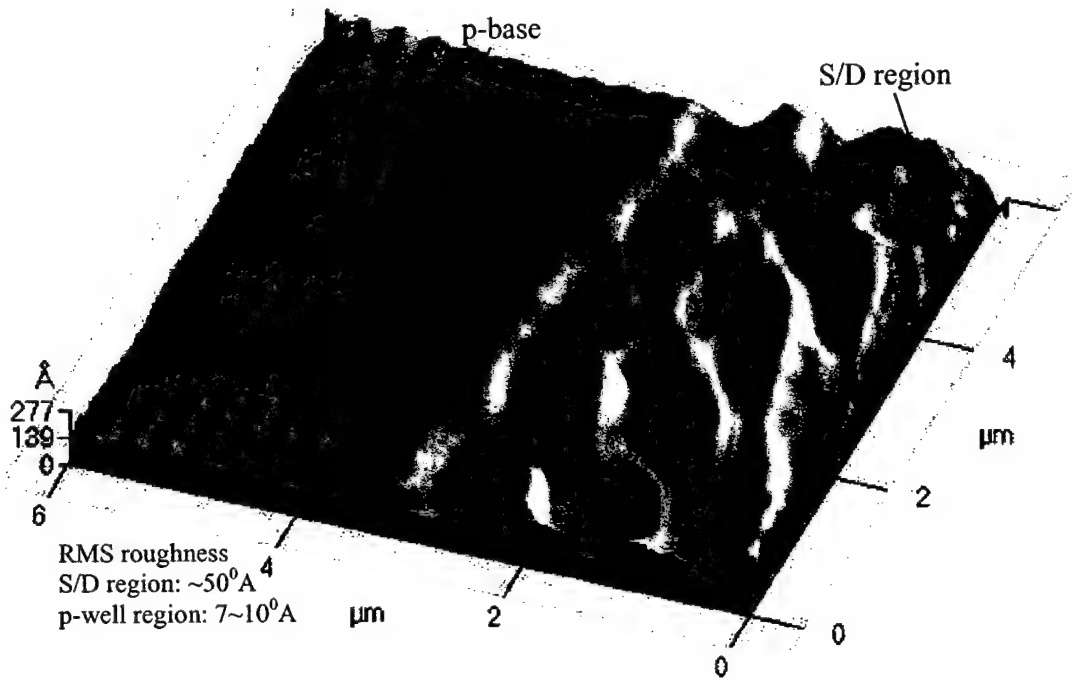


c) Wafer cross-section after the JTE implantation.

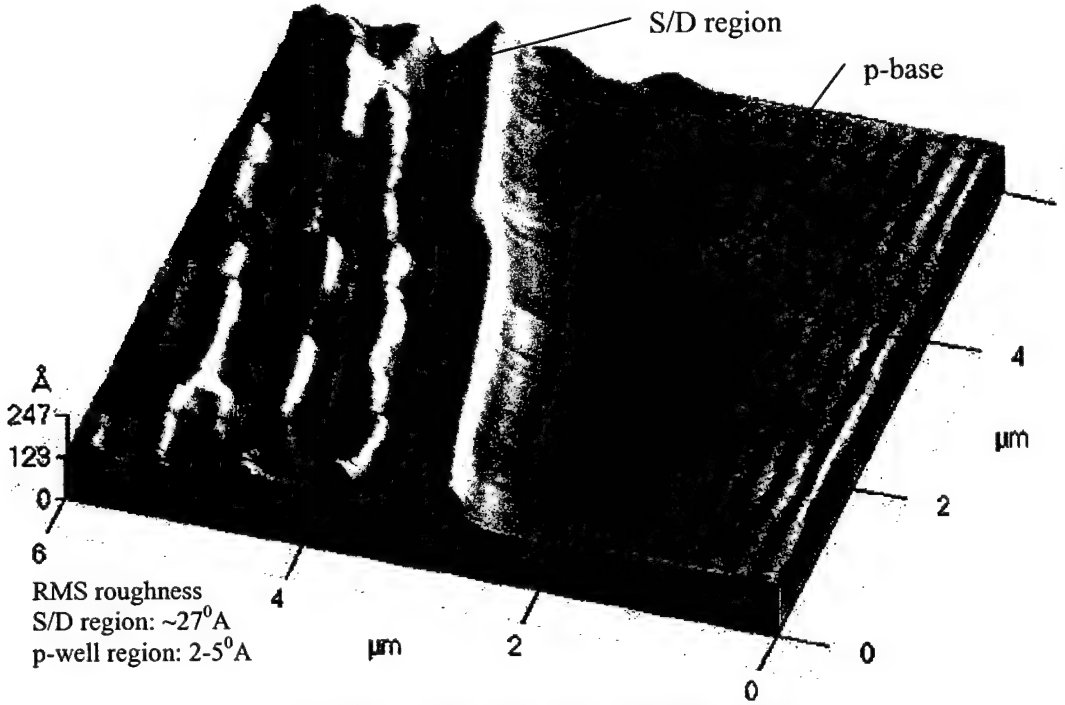
Fig. 7.20. Wafer photograph and cross-section after JTE implantations.

7.2.8 Implant Activation

Finding the optimum anneal temperature and anneal ambient to activate the implanted dopants is the topic of current research. While the nitrogen implantation in the source/drain regions can be 100% activated at a temperature $\leq 1500^0$C [58], of particular concern is activating the p-type Al accepter dopant, which requires an anneal temperature $> 1500^0$C to achieve > 50% activation [57], [60], [61]. SiC epitaxial layers are grown by "step controlled epitaxy", where growth takes place on the horizontal surfaces, but beginning at the wall of steps (lateral direction). Steps are formed when the growth surface is tilted 8^0 (4H-SiC) off-axis from the (0001) plane, and these steps contain the stacking information. Thus, the as-received SiC surface contains microscopic steps of approximately $10A^0$ (a single layer Si-C height ~$2.5A^0$). After the p-type implantation, implants are activated in excess of 1600^0C to obtain a high activation rate, and at this high temperature (close to SiC epigrowth temperature) sublimation of Si from the SiC surface can occur, causing small steps to coalesce into larger steps, thus increasing the step height (~$100A^0$) and separation of the steps, resulting in a surface roughness phenomenon called "step bunching" [13]. For SiC DMOS structures, the channel formed on this implanted surface can suffer from extremely low inversion channel mobility due to surface degradation after the high temperature anneal step. Capano et al. [15] investigated the surface roughness phenomenon in B and Al implanted 4H-SiC surfaces for different anneal ambient and anneal temperature. Experiments revealed that the surface roughness phenomenon can be minimized if the activation anneal of p-type implant is performed in a silane ambient, even at a high anneal temperature of 1700^0C. In order to find an optimum anneal condition, an experiment was performed by Dr. M. Satoh [9], where activation anneals in argon and silane ambients were investigated. Two 4H-SiC pieces were implanted with Al to form the p-base, together with a counter-doped nitrogen implant and a high dose nitrogen implantation to form the source of lateral FATFETs. The activation anneal was then performed at 1600^0C for 30 min in both argon and silane ambients. Figure 7.21 shows the AFM (atomic force microscopy) photographs of the annealed samples in argon and silane environments. The rms (root mean square)



a) Argon annealed p-base and S/D region



b) Silane annealed p-base and S/D region

Fig. 7.21. AFM microphotographs of the argon and silane anneal samples.

roughness measurements showed a factor of 2x higher value for the Ar annealed sample compared to the silane annealed sample. However, the inversion channel mobility extracted from the FATFET measurements for the argon annealed sample showed a slightly higher value (~25 cm^2/Vsec) compared to the SiH_4 annealed sample (18 cm^2/Vsec). This may be due to the fact that both samples were annealed in an EPIGRESS CVD reactor [62] where a silane overpressure from the SiC susceptor may have occurred during the argon anneal. In the experiment, both wafers were annealed with the thermal profile shown in Fig. 7.22.

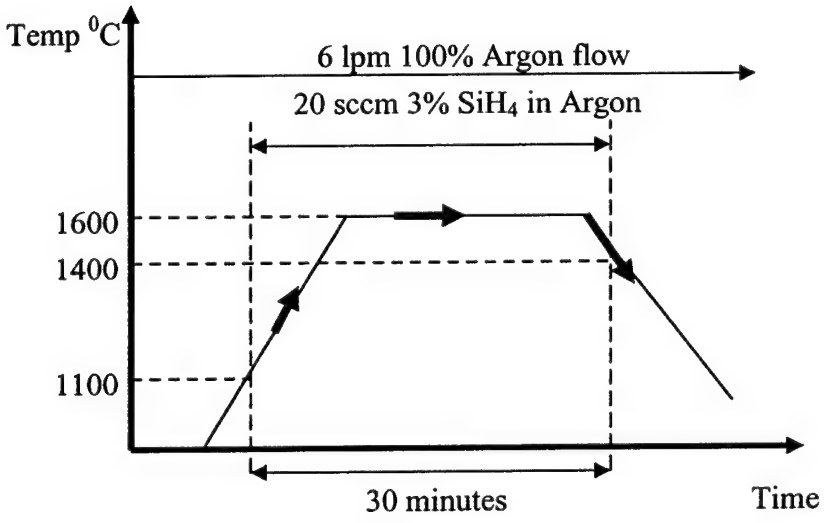


Fig. 7.22 Implant activation anneal conditions.

Figure 7.23 shows a test MOSFET after the implant activation anneal. In order to verify proper implant activation, high voltage measurements were performed on test diodes with JTE termination. A diode with a JTE width of 150 μm on the 4H-20 μm wafer was able to block 1679V, and this is shown in Fig. 7.24. A diode with JTE width of 150 μm on the

4H-50 μm wafer was able to block 4500V as shown in Fig. 7.25. The diodes were able to block high voltages several times without breaking down catastrophically.

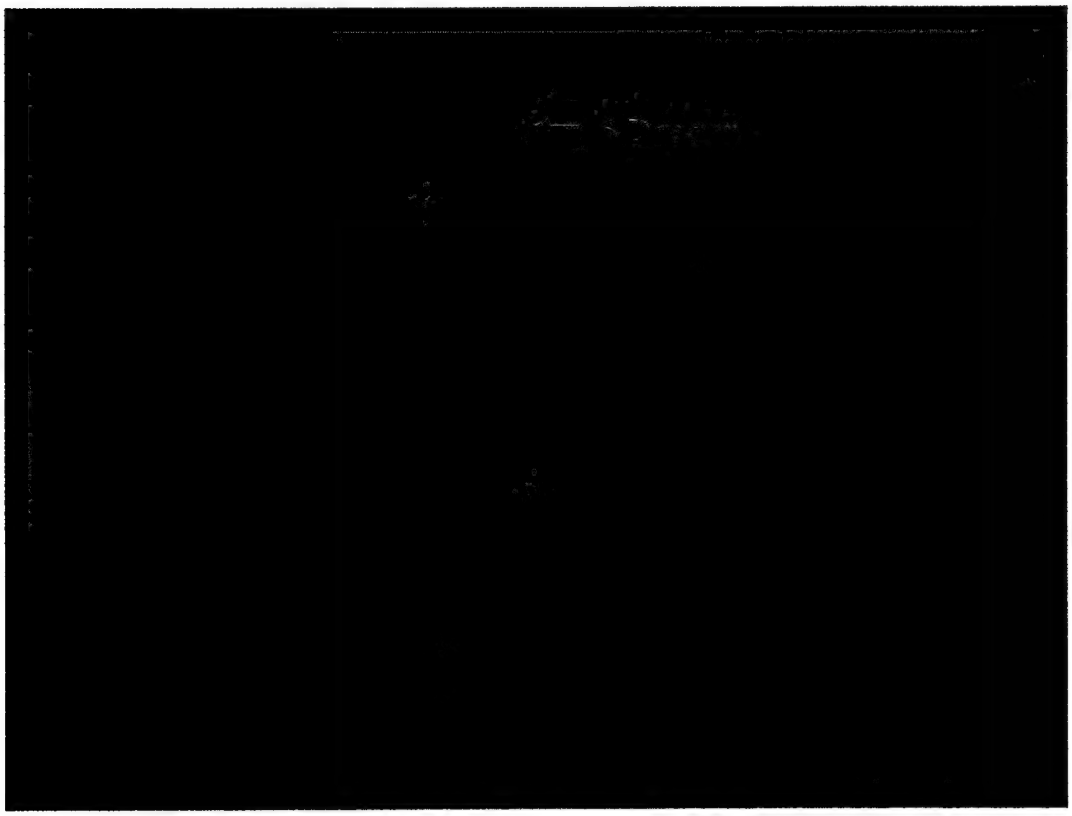


Fig. 7.23. Nomarski photograph of a 4H-50 μm sample after the 1600^0C implant activation anneal. Magnification X1000.

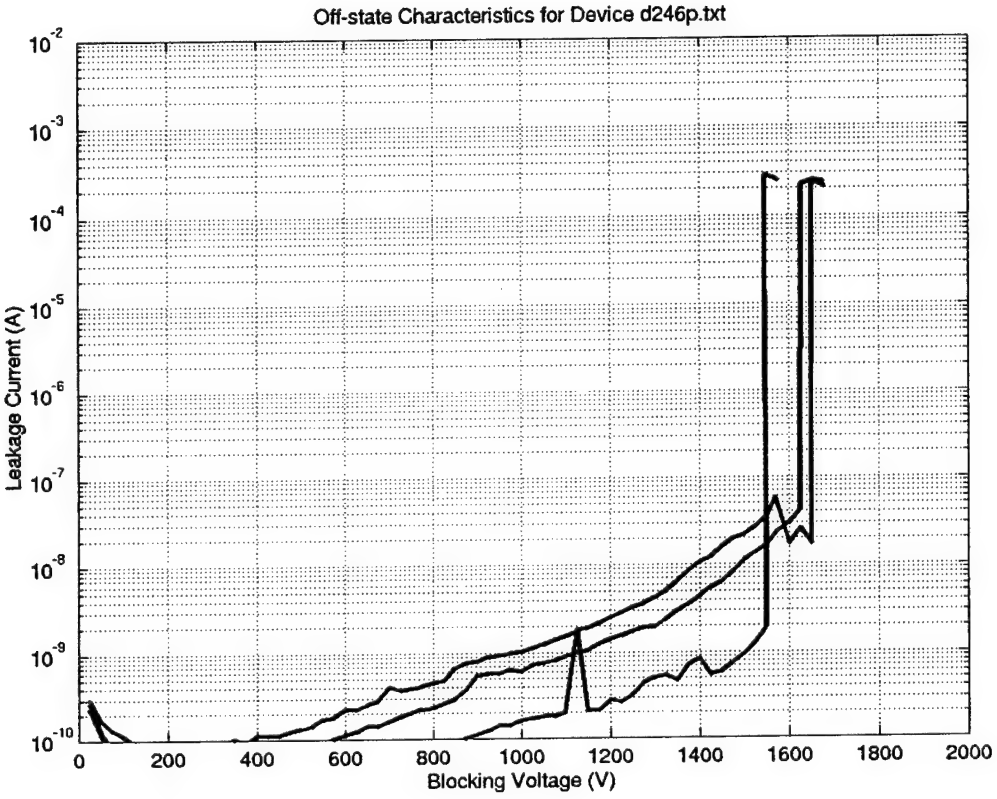


Fig. 7.24. Reverse blocking characteristics of a diode (diameter=60μm, JTE width=150μm) on the 4H-20μm wafer.

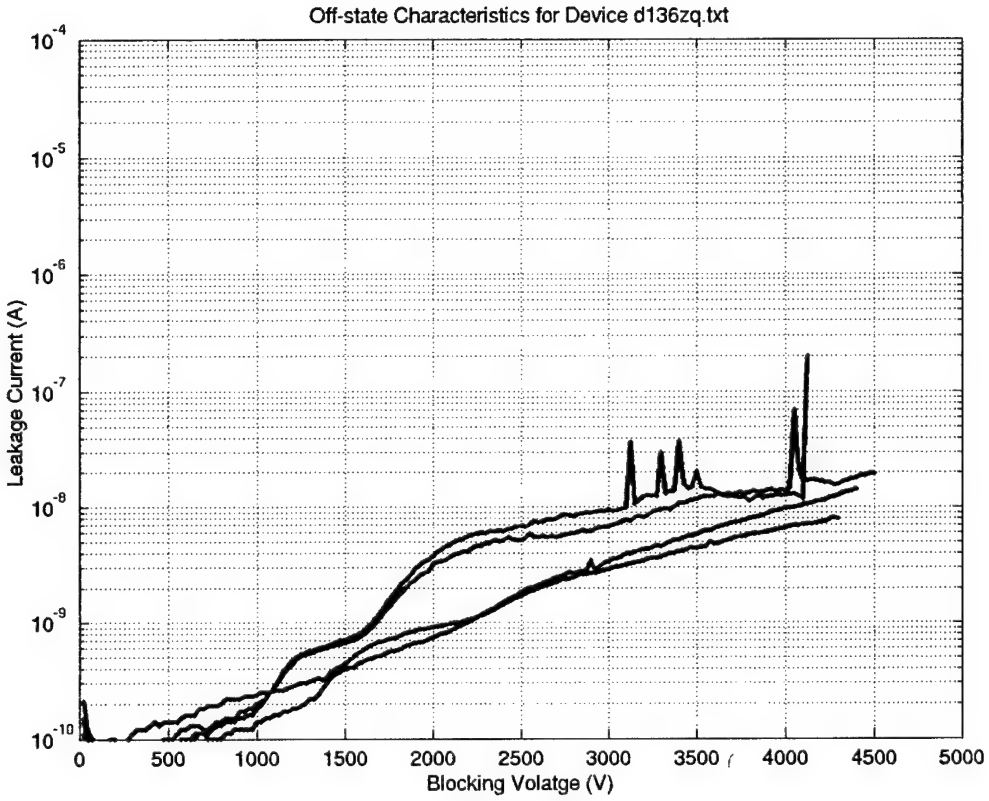


Fig. 7.25. Reverse blocking characteristics of a diode (diameter=60μm, JTE width=150μm) on the 4H-50μm wafer.

7.2.9 Gate oxidation, NO anneal, and gate patterning

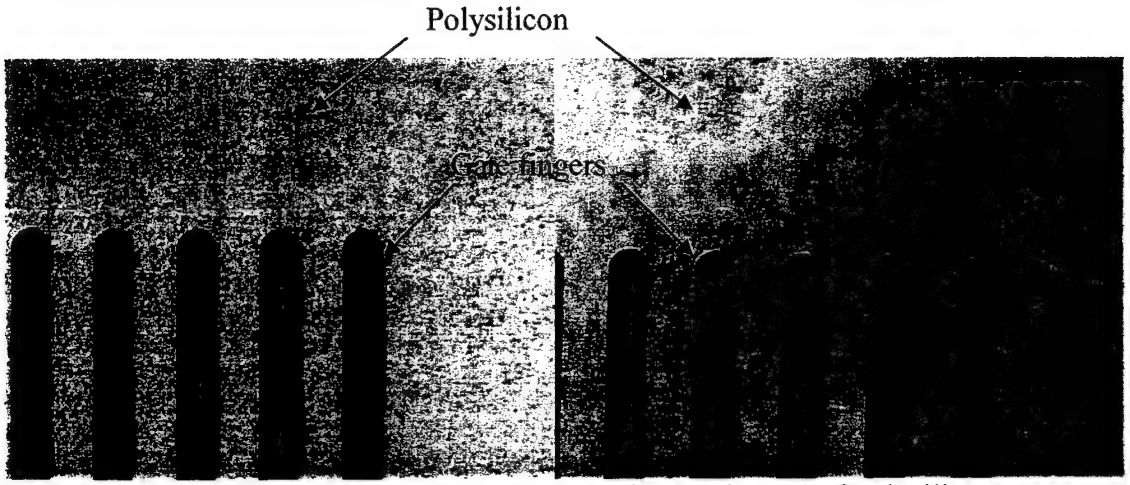
The wafers were RCA cleaned right before loading into a pyrogenic oxidation system. The gate oxidation was performed at 1150^{0}C for 1.5 hours with 25% O_2 and 15%

H_2 mixture and a 30 min in-situ Ar anneal at 1150^{0}C followed by the standard re-ox anneal at 950^{0}C for 2 hours. The water vapor content in a pyrogenic system can be controlled by changing the ratio of H_2 to O_2 gas flow rate, compared to a standard resistiance heated quartz-walled furnace, where water is flowed through deionized water at 95^{0}C to produce water vapor.

4H-SiC material has a high density of interface states at the upper half of the bandgap [63], which can significantly lower inversion channel mobility by charge trapping or by Coulomb scattering from these trapped electrons. Chung et al. of Auburn University [64] reported that by performing a post oxidation annealing step in nitric oxide (POA-NO), the interface trap density near the conduction band of 4H-SiC material can be reduced. Later, Chao-Yang Lu of Purdue University [65] verified that the POA-NO anneal can dramatically improve the inversion channel mobility of lateral MOSFETs formed on 4H-SiC. The field effect mobility value with NO anneal was ~35 cm^2/Vsec at a gate voltage of 20V, while without NO anneal it was 10~12 cm^2/Vsec. In the attempt to improve the inversion channel mobility of the DMOSFET's, the wafers were sent to Auburn University where they received a standard NO anneal (1 atm, 0.5 liter/min) at 1175^{0}C for 2 hours [66].

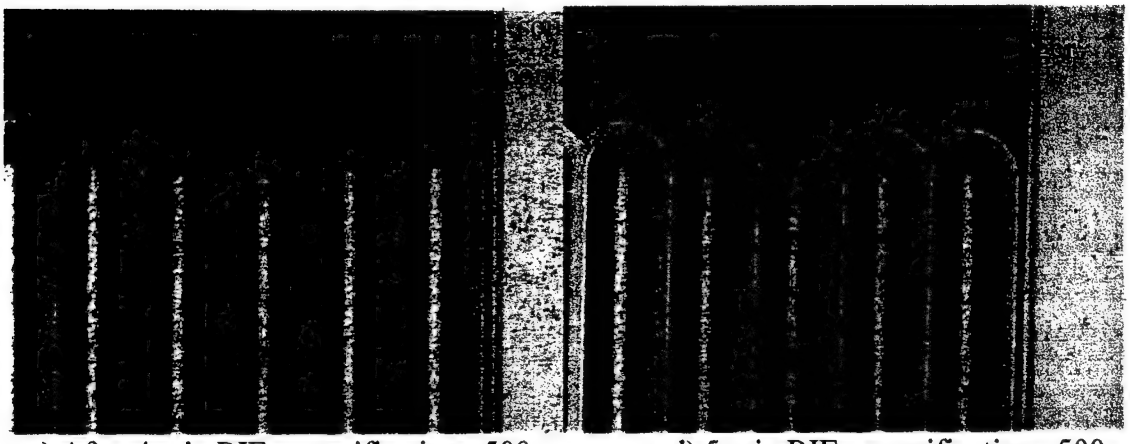
The wafers were piranha (1 H_2O_2:1 H_2SO_4) cleaned, and a 0.5μm thick polysilicon layer was deposited by LPCVD at 600^{0}C for 50 minutes to serve as the gate electrode. The polysilicon was then doped with phosphorus spin-on dopant, followed by a dopant drive-in step at 900^{0}C for 45 minutes. To check the conductivity of the polysilicon layer, 4-point probe measurements were performed, giving a sheet-resistivity of 122Ω/□ on the 4H-20μm (50 mm) and 45.6 Ω/□ for the 4H-50 (25 mm) wafer.

To pattern the polysilicon gates, a light-field AZ1518 photoresist Mask-6 was used. In order to prevent any gate oxide damage from the RIE process, the etch was performed at 30W power and at low DC bias of 45-50V with SF_6 gas (10sccm). Figure 7.26 shows a photograph of the 4H-50μm wafer after different etching times.



a) 0 min RIE, magnification x500

b) After 2 min RIE of polysilicon, magnification x500



c) After 4 min RIE, magnification x500.

d) 5 min RIE, magnification x500.

Fig. 7.26. RIE of polysilicon gate.

7.2.10 Contact metal deposition

The backside polysilicon and oxide on the wafers were removed by covering the front side with AZ1518 photoresist. A photoresist Mask-8 was used to remove oxide from the contact areas. This also removed oxide in the p^+ contact areas, as in our process the Ni always covers the Al. An Ni/Al (200^0A/500^0A) layer was deposited by e-beam evaporation and liftoff lithography using p^+ Mask-7, and a 500^0A Ni layer was deposited and defined by liftoff lithography using n^+ Mask-8. The drain contact was formed by depositing 2000^0A of Ni on the backside. Figure 7.27 show device photographs after the front contact metal depositions and a device cross-section at this point. All contacts were annealed at 850^0C for 2 min in vacuum (4H-20μm). A 7000^0A Au layer was deposited and defined by liftoff lithography using Mask-8 to serve as the top metal.

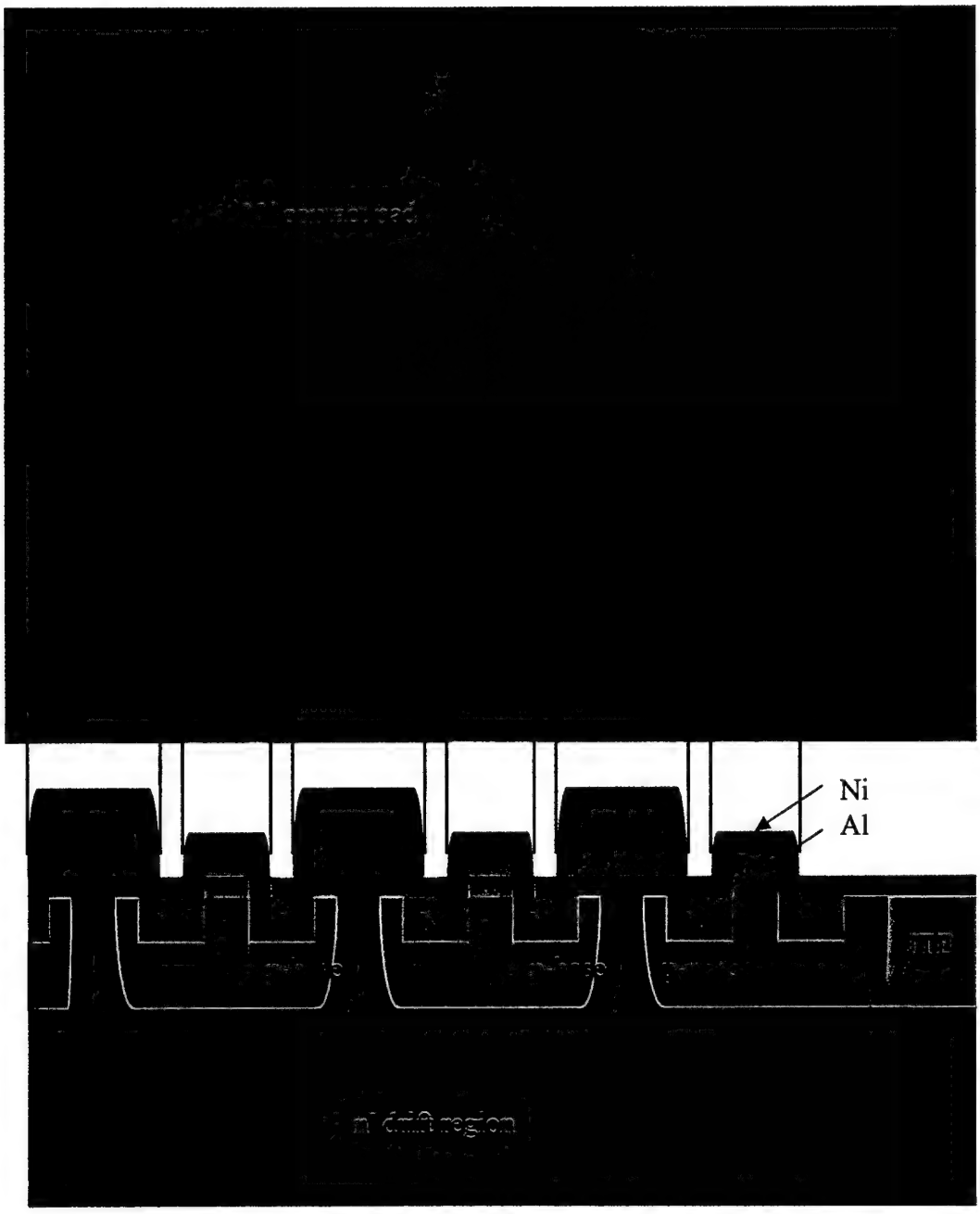


Fig. 7.27 A 4H-20μm short channel DMOSFET with front contacts and also showing final device cross-section.

8. EXPERIMENTAL RESULTS ON SHORT CHANNEL COUNTER DOPED SELF ALIGNED 4H-SIC DMOS DEVICES

8.1 Device Performance during the On and Off-State

The on-state I-V measurements of the self-aligned short channel counter-doped DMOS transistors were performed using an HP4156 parameter analyzer. With the source and base grounded, the drain characteristics were obtained by applying positive voltages to the drain and gate. The gate oxide thicknesses were extracted from n^- MOS-capacitors using an HP4284 precision LCR meter. The oxide thicknesses for the 4H-20μm and 4H-50μm samples were ~425^0A and ~408^0A respectively. The specific on-resistances were then calculated from the linear portion of the I-V plot. The off-state characteristics were measured using a PS350 Stanford power supply along with a Fluke 5840 digital multimeter capable of measuring voltages up to 5kV. The leakage current through the device was monitored with gate and source grounded, and applying a reverse (positive) voltage to the drain. The on-state and off-state I-V characteristics of DMOSFETs on the 4H-20μm sample after contact anneal are shown in Fig. 8.1 through Fig. 8.6. The I-V characteristics for devices with a 2-3 design rule and with L_{JFET} of 4, 6 and 8μm are shown in Fig. 8.1, Fig. 8.2 and Fig. 8.3 respectively. The specific on-resistances calculated from the linear slope of the I_d-V_{ds} plot through the origin were 26.9 mΩ-cm^2, 28 mΩ-cm^2, and 26.6 mΩ-cm^2 respectively. The off-state blocking voltages of the devices were 1530V, 2000V and 1820V respectively. The devices were able to block high voltages several times without breaking down catastrophically or reaching the 1mA limit.

The on-state drain characteristics of devices with 3-5 design rules and with L_{JFET} of 4, 6 and 8μm are shown in Fig. 8.4, Fig. 8.5 and Fig. 8.6 respectively. The specific on-resistances calculated were 39.9 mΩ-cm^2, 31.8 mΩ-cm^2, and 36.4 mΩ-cm^2 respectively.

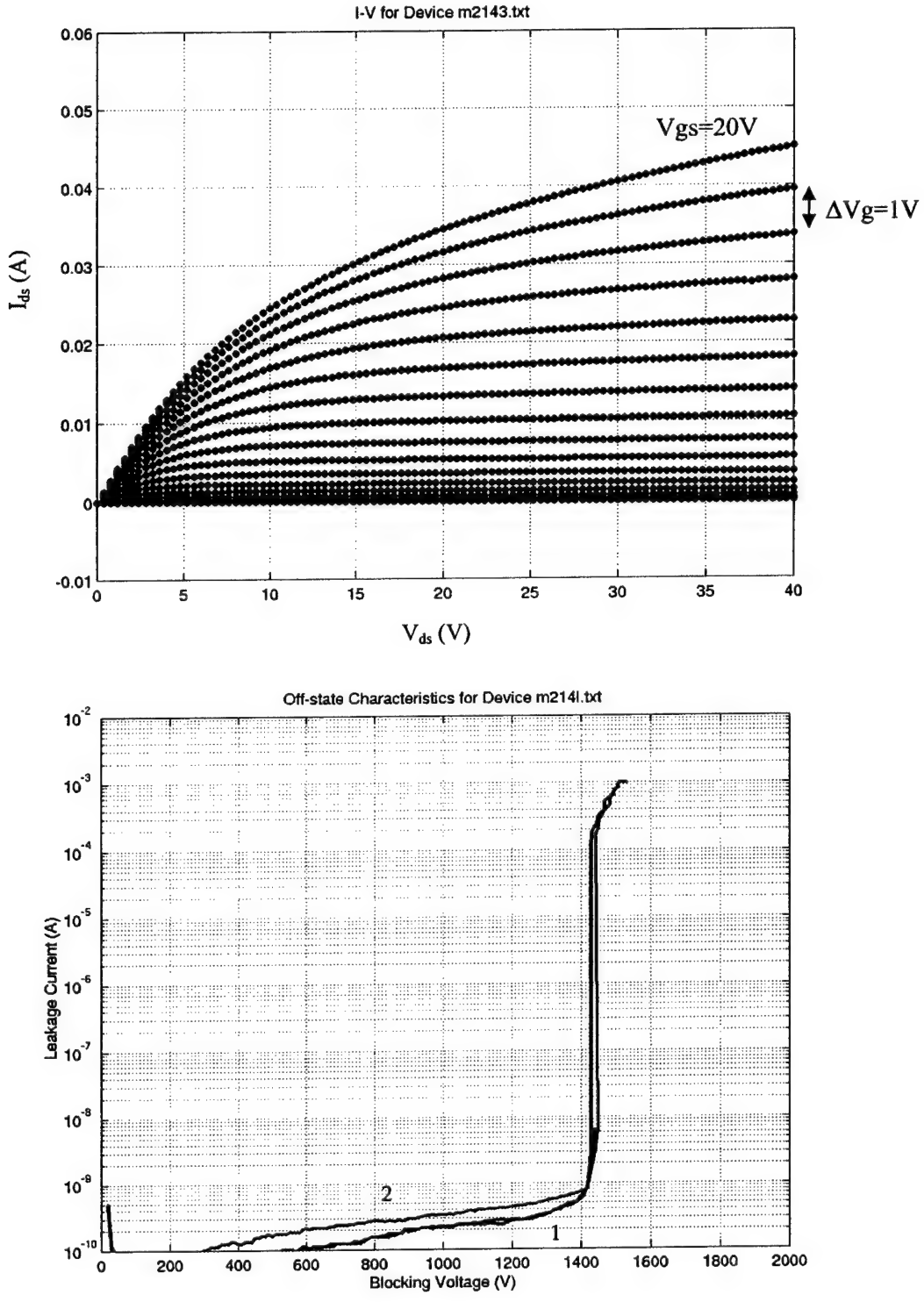


Fig. 8.1. Forward and reverse characteristics of a DMOSFET on 4H-20μm with 2-3 design rules, L_{JFET}=4μm and active area A=$1.04 \cdot 10^{-4}$ cm^2. Curves 1 and 2 represent repeated high voltage measurements on the same device.

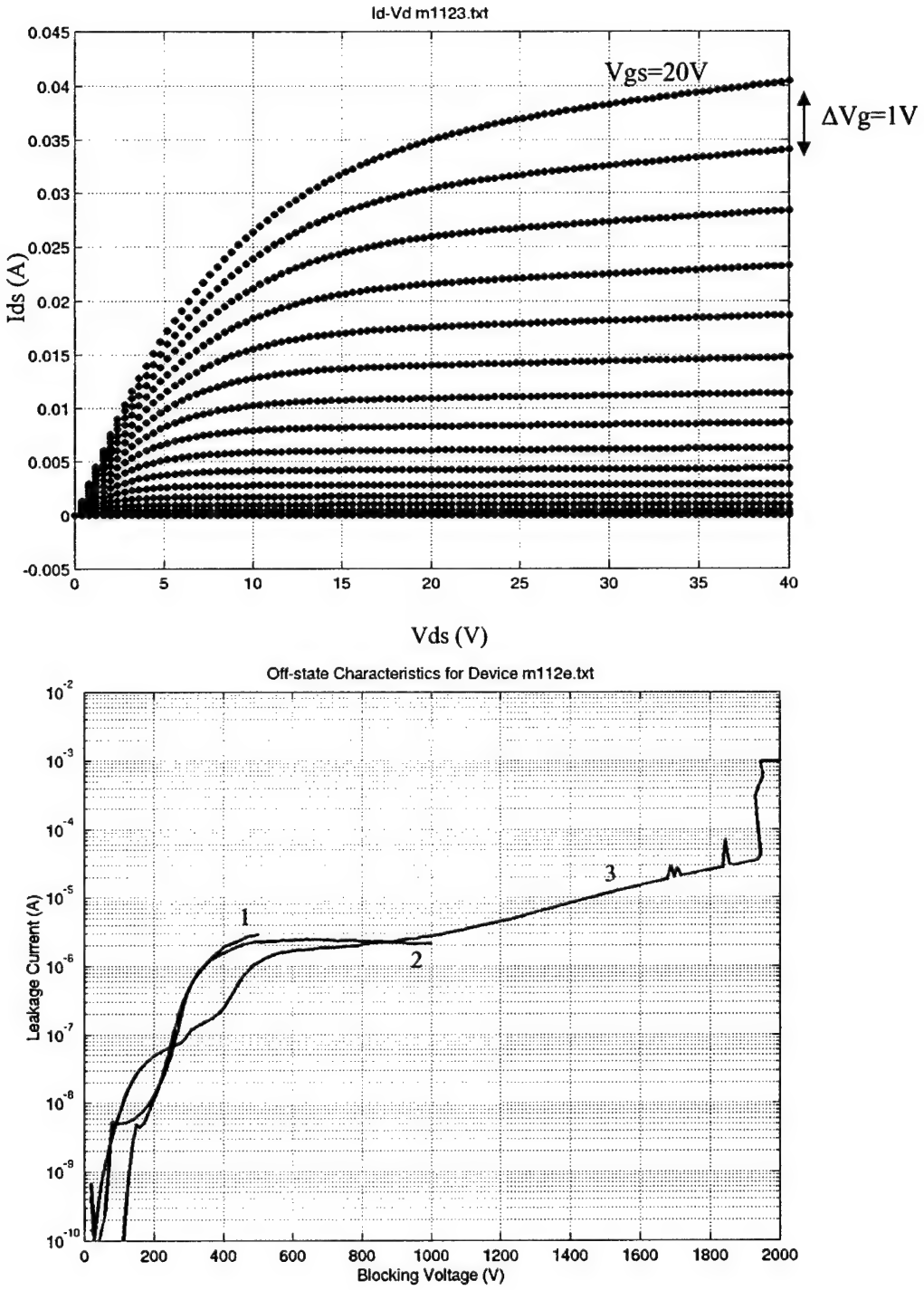


Fig. 8.2 Forward and reverse characteristics of a DMOSFET on 4H-20μm with L_{JFET}=6μm and A=$1.144 \cdot 10^{-4}$ cm^2 with 2-3 design rules. Curves 1, 2, and 3 represent repeated high voltage measurements on the same device.

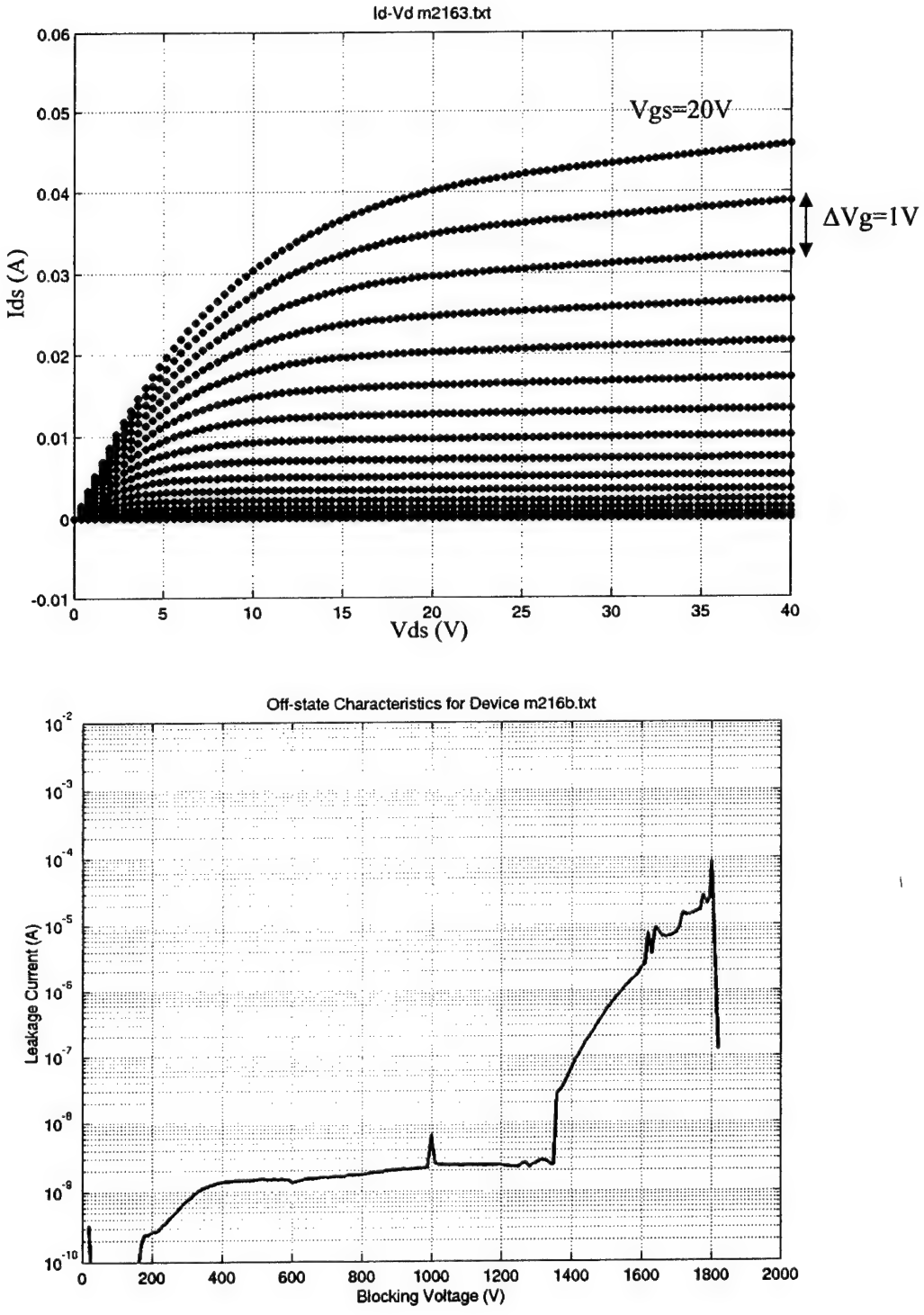


Fig. 8.3. The forward and reverse I-V characteristics of a DMOSFET on 4H-20μm sample with 2-3 design rules, L_{JFET}=8μm and A=1.248·10^{-4} cm^2.

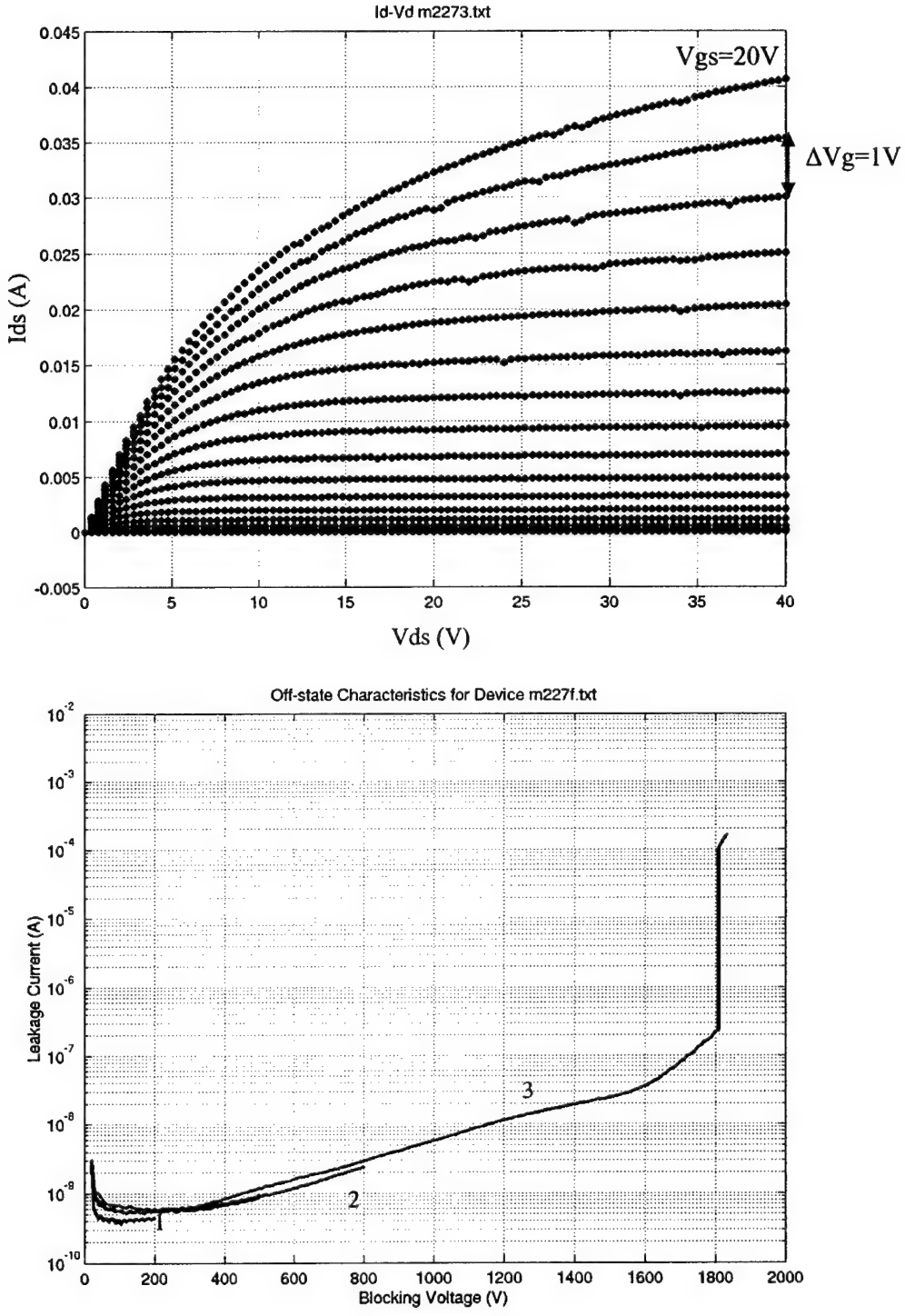


Fig. 8.4. Forward and reverse I-V characteristics of a DMOSFET on 4H-20 μm sample with 3-5 design rules L_{JFET}=4 μm and A=1.456·10^{-4} cm^2. Curves 1, 2, and 3 represent repeated high voltage measurements on the same device during the off-state.

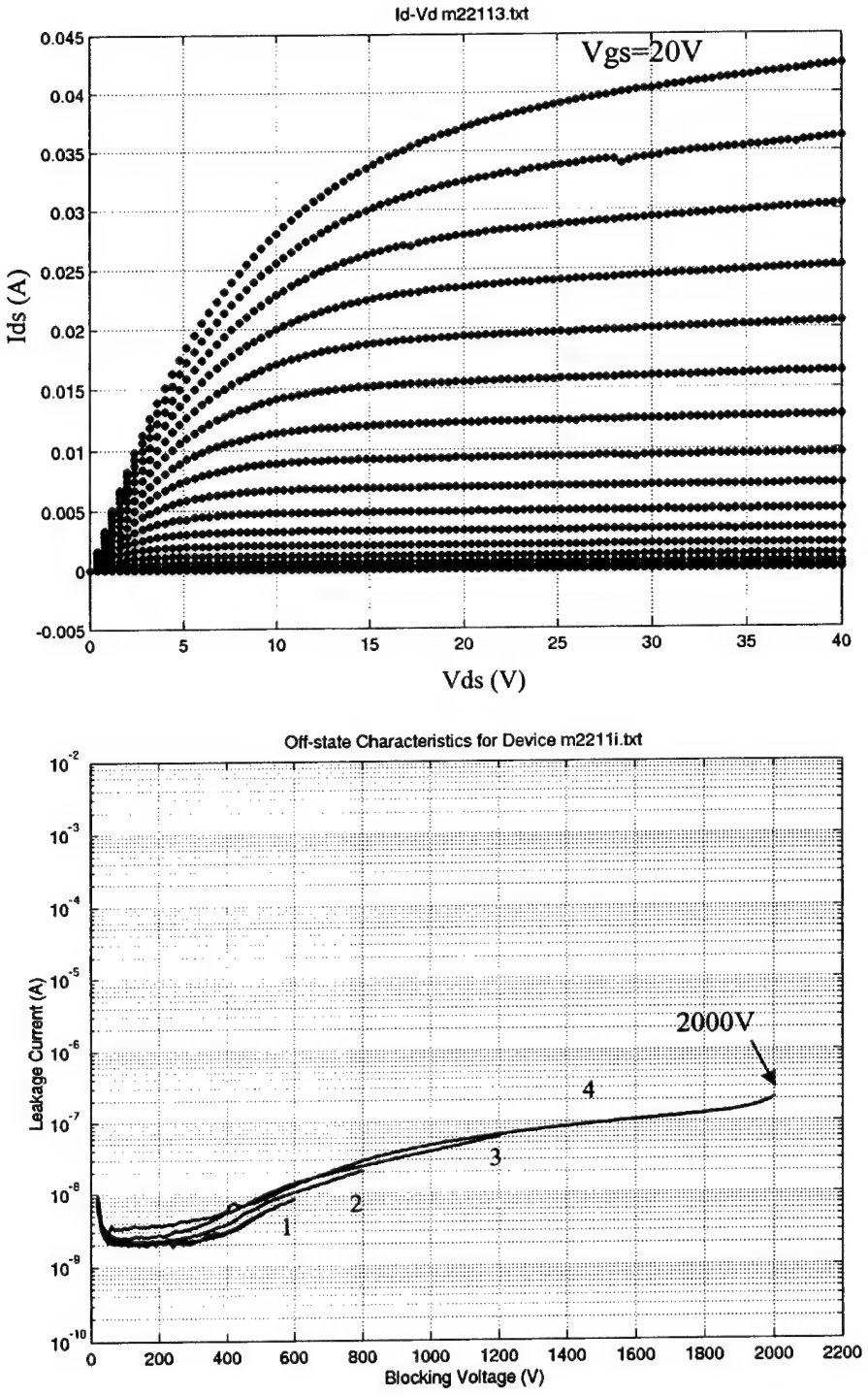


Fig. 8.5. Forward and reverse I-V characteristics of a DMOSFET on 4H-20μm sample with 3-5 design rules, L_{JFET}=6μm and A=1.56·10^{-4} cm^2. Curves 1, 2, 3, and 4 represent repeated high voltage measurements on the same device during the off-state.

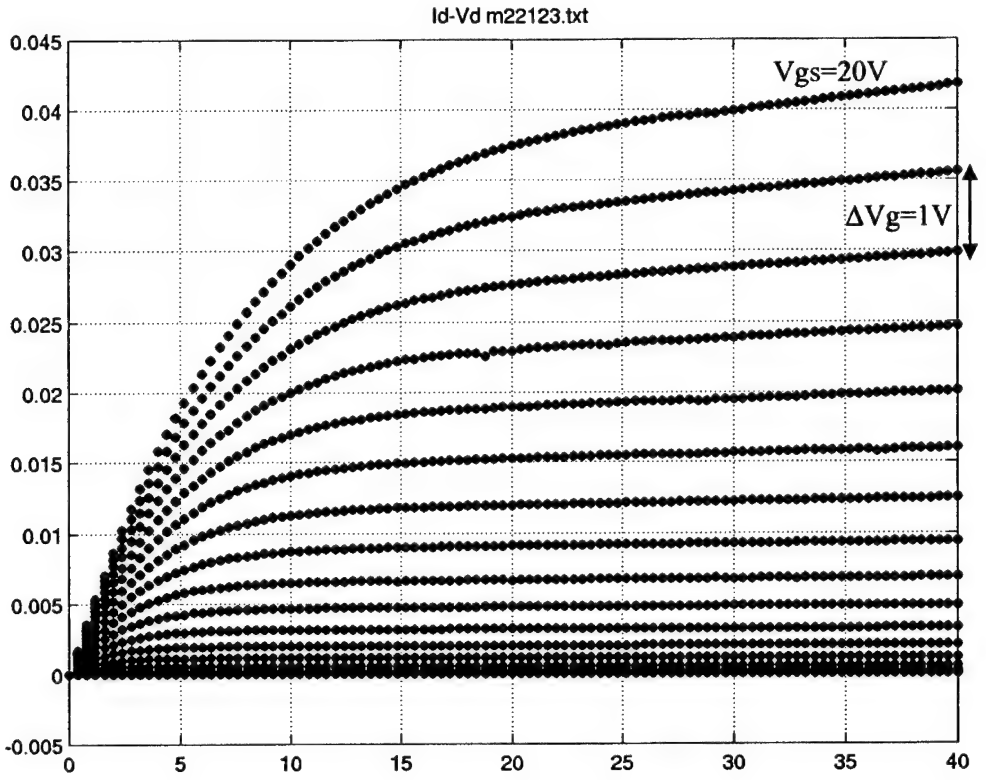


Fig. 8.6. Forward I-V characteristics of a DMOSFET on 4H-20μm sample with 3-5 design rule and L_{JFET}=8μm. The active area A=1.664·10^{-4} cm^2.

The breakdown voltages for the first two devices (3-5 design) were 1820V and 2000V respectively. The specific on-resistances for the short channel devices on the 4H-20μm sample were not as low as expected. However, they represent the best performing DMOS transistors to date on a 20μm thick drift region. The lowest specific on-resistance value obtained was 26.6 mΩ-cm^2 with L_{JFET}=8 μm with (2-3 design rules) and the highest blocking voltage achieved was 2000V with L_{JFET}=6 μm, which is 67% of the theoretical blocking voltage for a 20 μm thick drift region. The blocking strength did not change after the poly dopant drive-in (900^{0}C) or the contact anneal (850^{0}C) step.

8.2 Field-Effect Mobility, Threshold Voltage, Effective Mobility, and TLM Measurements

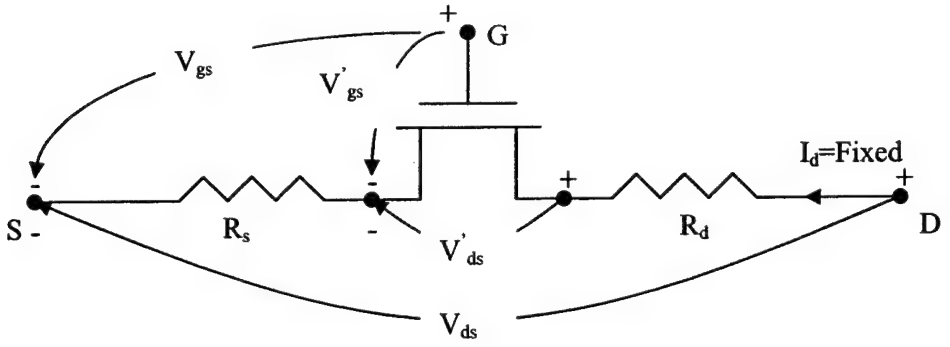


Fig. 8.7. A MOSFET with source and drain resistance. This model was used to measure the inversion channel mobility.

To determine the inversion channel mobility accurately, long channel FATFETs with channel lengths (L_{ch}) of 50 μm, 80 μm, 100 μm, and 140 μm were measured. The schematic representation of the MOSFET used to calculate the channel mobility (μ_{ch}) is shown in Fig. 8.7. The field-effect mobility was extracted using a "constant-current method" [65]. The drain current of a lateral MOSFET in the linear region is given as:

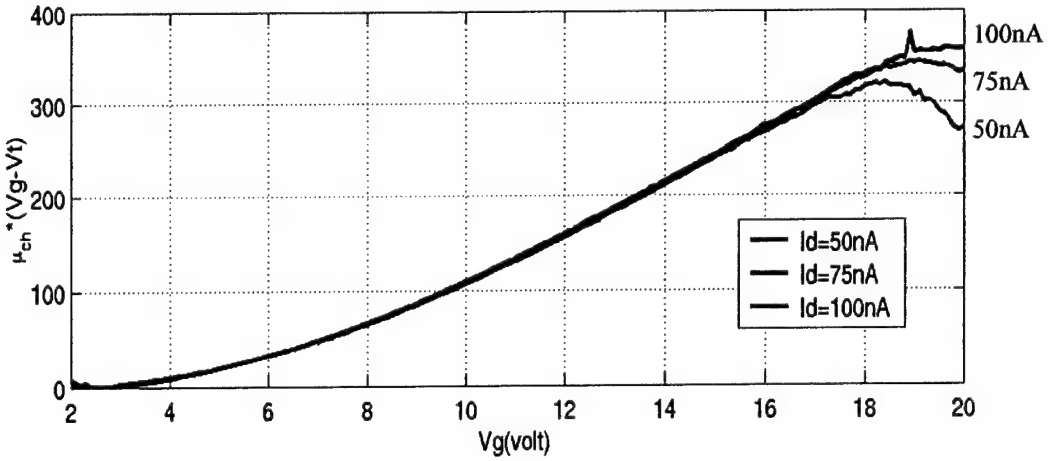
$$I_d = \frac{\mu_{ch} C_{ox} W (V_{gs} - I_d R_s - V_t)(V_{ds} - I_d (R_s + R_d))}{L_{ch}} \qquad (8.1)$$

where I_d is the drain current, C_{ox} is the capacitance per unit area, W is the channel width, R_s is the source resistance, R_d is the drain resistance, V_{gs} is the gate voltage, V_t is the threshold voltage, and V_{ds} is the drain voltage. The extraction of channel mobility becomes difficult when the source and drain resistance is large, and particularly if their I-V characteristics are non-ohmic. In this method a constant drain current (I_d) is maintained and the voltage drop from source to drain (V_{ds}) is monitored as the gate voltage (V_{gs}) is varied. With I_d fixed, voltage drop across the source and drain contacts should be constant. The measured voltage drop ($V_{ds}=V_s+V_d+V_{ch}$) is then plotted versus the channel length (L_{ch}) as given by equation 8.2.

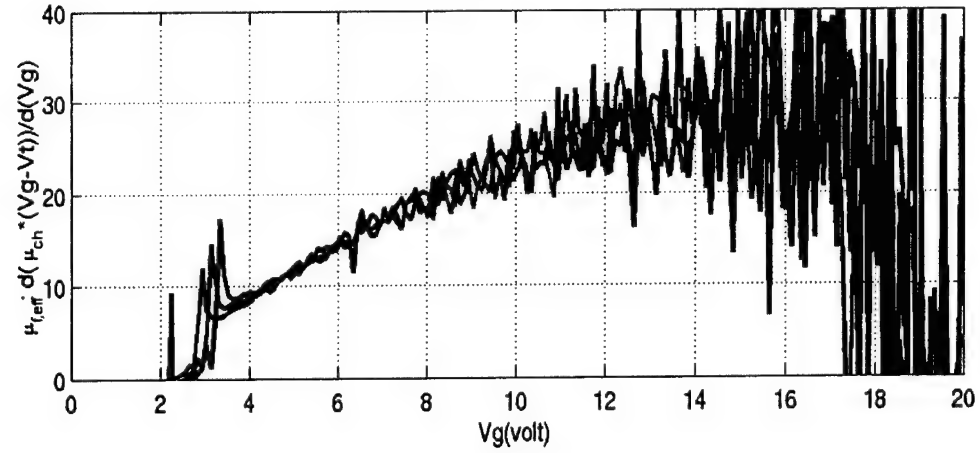
$$V_{ds} = \frac{L_{ch} I_d}{\mu_{ch} C_{ox} W (V_{gs} - I_d R_s - V_t)} + I_d (R_s + R_d) \qquad (8.2)$$

The y-axis intercept of the linear fit to the data gives the actual voltage drop in the source and drain regions, and the slope then gives the electric field across the channel (V_{ds}/L_{ch}). From the slope (see equation 8.2), neglecting the I_dR_s voltage drop (assuming V_{gs}>> I_dR_s), we can determine a mobility x gate voltage product $\mu_{ch}x(V_{gs}-V_t)$ for the measured FATFETs. Figure 8.8a shows a plot of $\mu_{ch}x(V_{gs}-V_t)$ versus the gate voltage V_{gs}. By differentiating $\mu_{ch}x(V_{gs}-V_t)$ with respect to V_{gs}, the field-effect mobility can be extracted, and Fig. 8.8b shows the resulting field-effect mobility plot for the 4H-50 μm sample. Figures 8.9a and b show the field-effect mobility vs. applied gate voltage plots for the 4H-20 μm and 4H-50 μm sample respectively, obtained by the constant-current technique. The maximum field-effect mobility for the 4H-20 μm sample is 18 cm^2/Vsec and for the 4H-50 μm sample the maximum field-effect mobility is 30 cm^2/Vsec at a gate voltage of 18V. The NO anneals and counter-dopants in the channel have significantly improved the inversion channel mobility for both samples. Although both samples were processed together right up to contact metal deposition, the 4H-50 μm sample showed two times higher mobility value compared to the 4H-20μm sample. The threshold voltage V_T for the 4H-20 μm sample was ~6V, and V_T for the 4H-50 μm sample was ~4V, which indicates a slightly higher buried-channel implant in the 4H-50 μm sample. This may explain the higher mobility in the 4H-50 μm sample.

The threshold voltage was extracted from the linear extrapolation of the I_d-V_{gs} plot with the drain voltage at 50mV. Lateral MOSFETs with channel lengths of 3, 5, 10 and 20 μm and FATFETs with longer channel lengths of 50, 80, 110, and 140 μm were measured. The threshold voltage for the 4H-20 μm sample varied between 5.6 to 7.5V and for the 4H-50 μm sample the threshold voltage varied between 2.4 to 3.9V from device to device. The threshold voltage did not show any systematic variations across the sample. However, the threshold voltage varied with channel length and decreased when the channel lengths were made smaller.

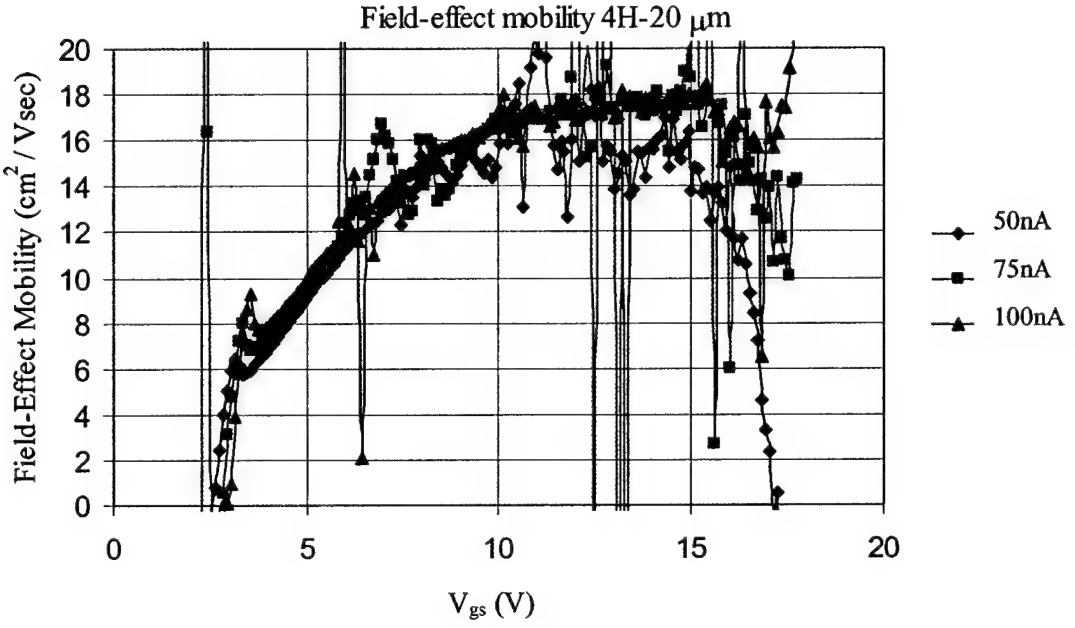


a)

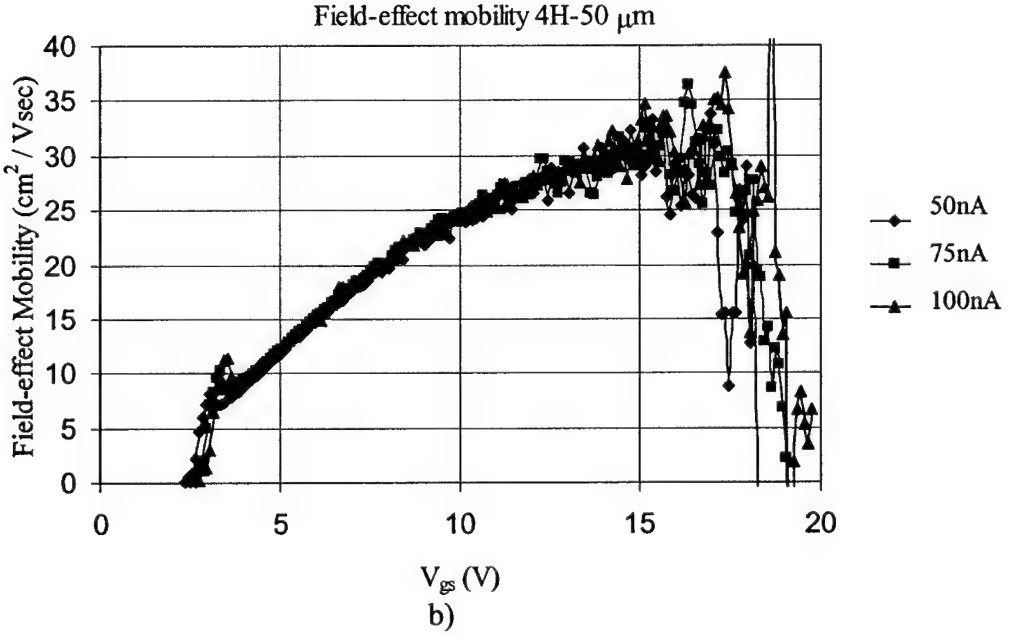


b)

Fig. 8.8 a) Mobility * gate voltage product versus gate voltage, and b) field-effect mobility versus gate voltage for the 4H-50μm sample. The measurements were performed by the "constant-current method"[65].



a)



b)

Fig. 8.9. Field-effect mobility versus gate voltage for the 4H-20 μm and 4H-50 μm samples measured by the " constant-current technique" [65].

Once the threshold voltage is known, the effective mobility is then determined from the slope of equation (8.2) measured by the "constant-current" technique. Figures 8.10 a and b show the effective mobility and field-effect mobility plots for the 4H-20 μm and 4H-50 μm respectively. For calculating the effective mobility for the 4H-20 μm sample, a V_t of 6V was assumed and for the 4H-50 μm sample, a V_t of 4V was assumed. The maximum value of effective mobility is 18 cm^2/Vsec at a gate voltage of 18V for the 4H-20 μm sample. For the 4H-50 μm sample, the effective mobility peaks at 25 cm^2/Vsec at a gate voltage of 18V and decreases to 23 cm^2/Vsec at a gate voltage of 20V.

The source (n^+) and base (p^+) sheet resistances and the ohmic contact resistances were measured by the TLM (Transfer Length Method) method. Figures 8.11 and 8.12 show the TLM measurements of the contact resistivity and sheet resistance for the source and base regions respectively on the 4H-20μm sample after the 850^0C vacuum anneal for 2 minutes. The lowest sheet resistance and contact resistivity values for the n^+ region were measured to be $2.04 \cdot 10^3$ Ω/□ and $\rho_c = 8.18 \cdot 10^{-4}$ Ω-cm^2 respectively. The sheet resistivity and contact resistance values were not uniform, and the highest values measured were $\rho_s = 2.21 \cdot 10^3$ Ω/□ and $\rho_c = 1.38 \cdot 10^{-3}$ Ω-cm^2 respectively. The contact resistance values were two to three orders of magnitude higher compared to the best value of $5 \cdot 10^{-6}$ Ω-cm^2 (where the Ni contacts to an n- type 6H-SiC epilayer ($7.8 \cdot 10^{18}$ cm^{-3}) were annealed at 950^0C for 2 min in vacuum) reported by Crofton et al. [67].

The sheet resistance for the p-type contact region was calculated to be $2.6 \cdot 10^4$ Ω/□ and the contact resistivity measured was $2.1 \cdot 10^{-2}$ Ω-cm^2. The contact resistance values for the p-type region were also two orders of magnitude higher compared to the best value of $1.5 \cdot 10^{-4}$ Ω-cm^2 (where the Al/Ti contacts to a p-type 4H-SiC epilayer ($7 \cdot 10^{18}$ cm^{-3}) were annealed at 1000 for 2 min in vacuum) reported by Crofton et al. [68].

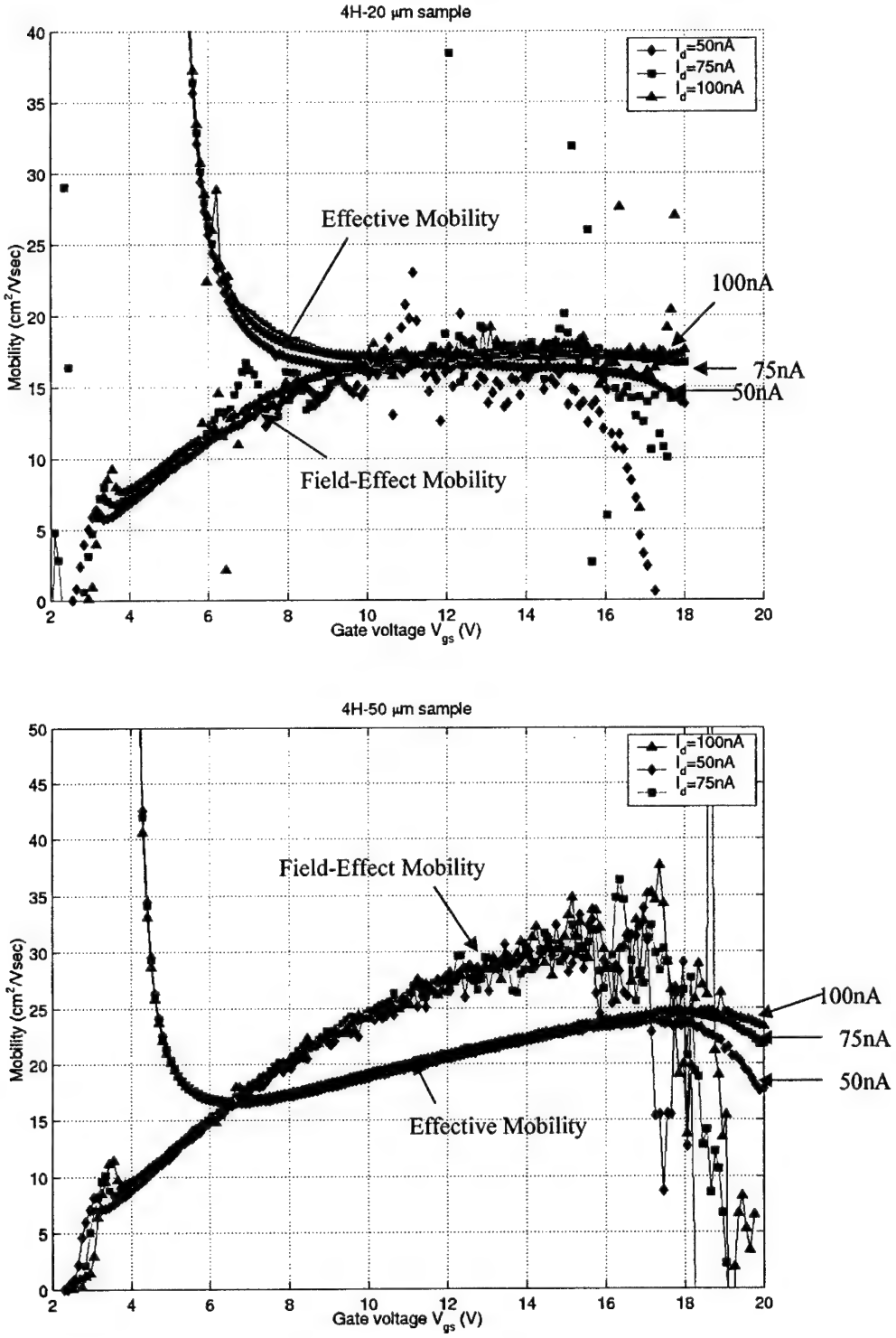
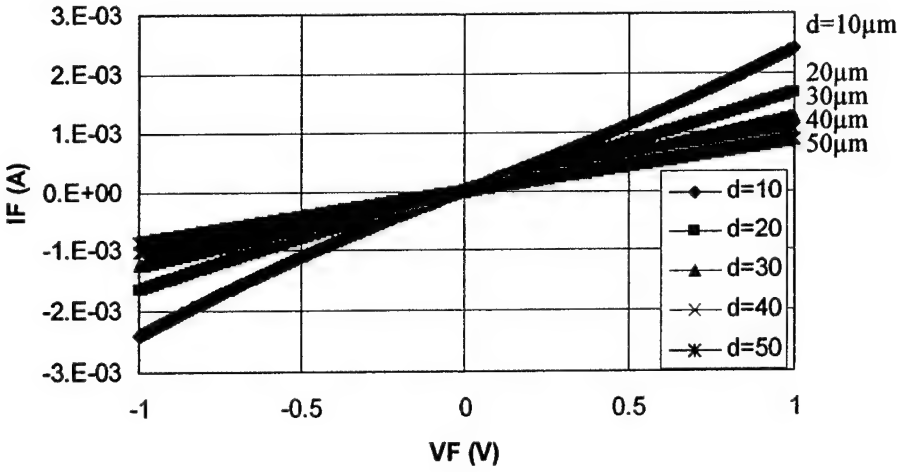
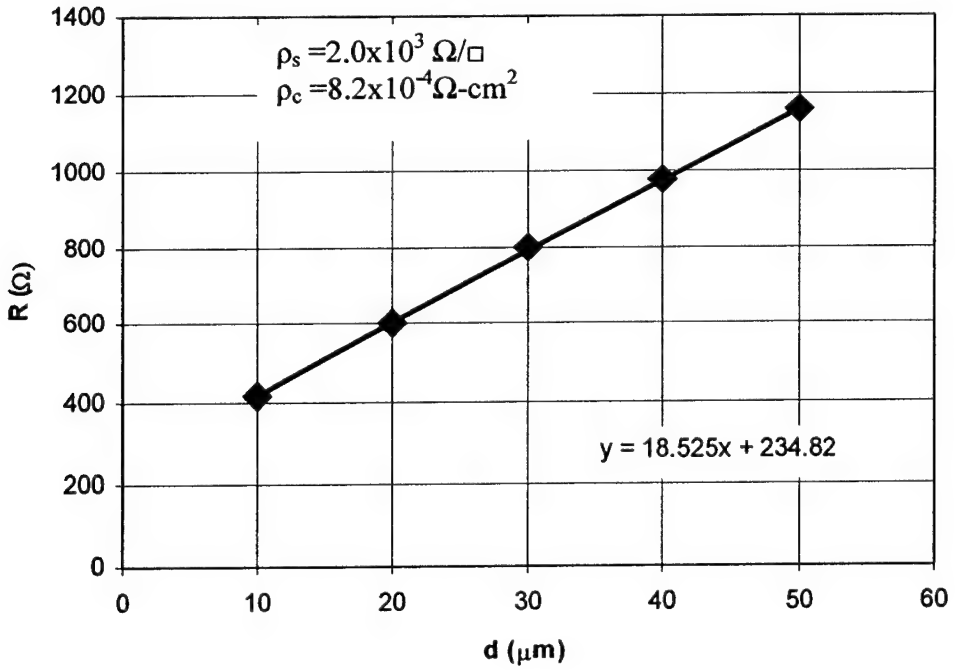


Fig. 8.10. Effective and field-effect mobility calculated by the constant-current technique [65]. The upper plot is for the 4H-20 μm sample, and the lower plot is for the 4H-50 μm sample.

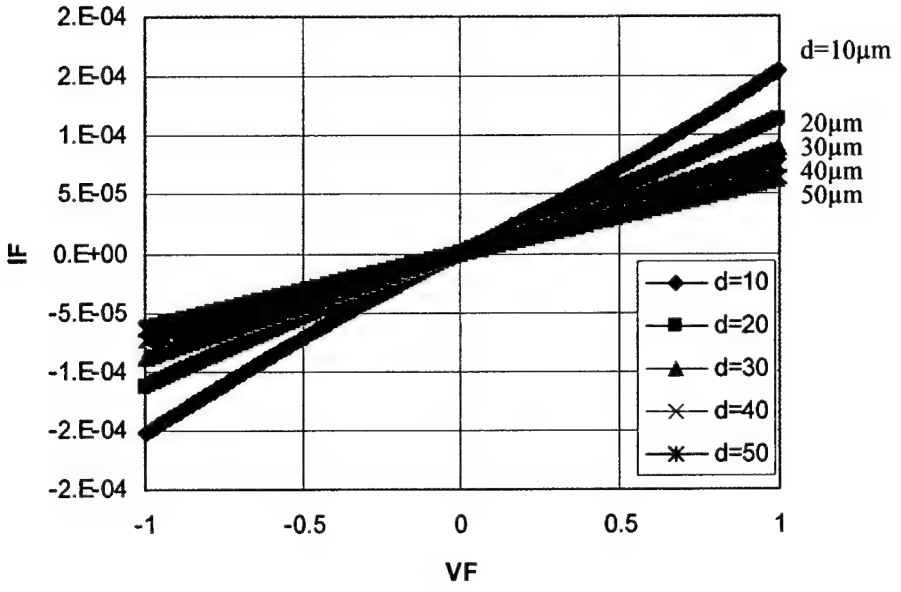


a) I-V characteristics of the measured TLM structures.

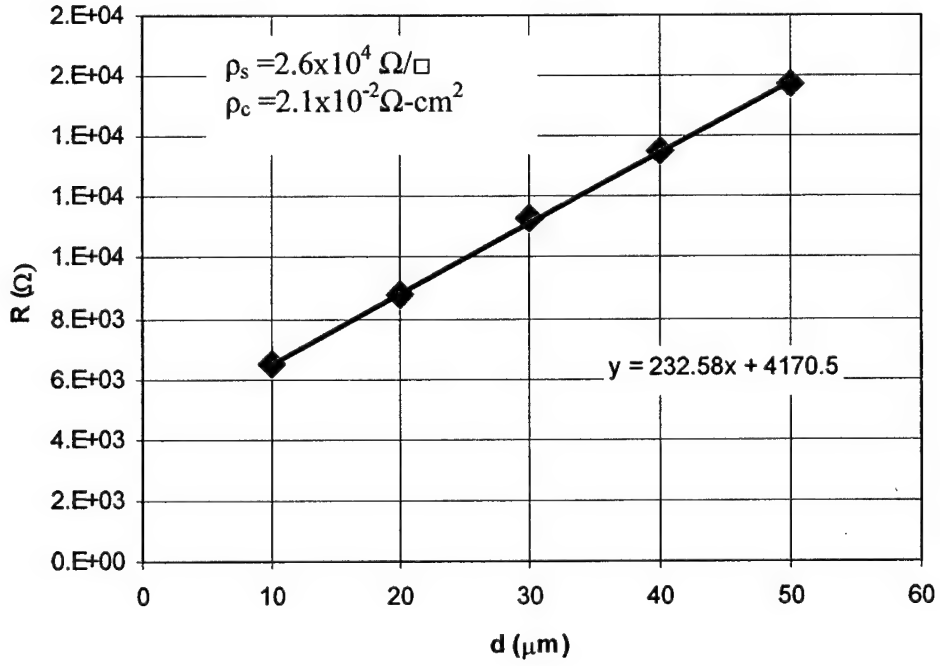


b) TLM data for the n^+ source region.

Fig. 8.11. TLM measurements of the contact resistivity and sheet resistance for the n-type source region on the 4H-20μm sample.



a) I-V characteristics of the TLM structures in p^+ base region.



b) TLM data for the p^+ base region.

Fig. 8.12. TLM measurements of the contact resistivity and sheet resistance for the p^+ base contact implanted regions on the 4H-20μm sample.

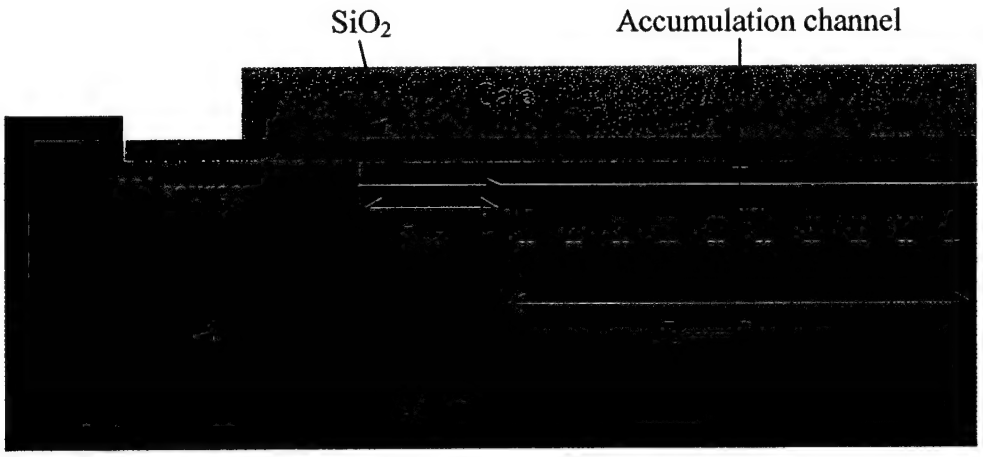
8.3 Modeling the Specific On-Resistance of the DMOS Structure on the 4H-20μm Piece

To reduce the channel resistance we have reduced the channel length to 0.5μm, and to reduce the overall specific on-resistance by reducing the device area, we have used self-aligned source and base contacts. Analysis of the results shows that, although the channel resistance has gone down, the overall specific on-resistance has not gone down as expected. To identify the dominant resistance contributor to the total on-resistance of the DMOS structure, we break down the specific on-resistance into the source resistance, the channel resistance, the accumulation channel resistance, the JFET resistance, and the drift region resistance. In this section, the "accumulation channel resistance" is included in the model, because we feel that without this resistance our previous analysis (in section 5.2) may have given an optimistic prediction of the specific on-resistance values for the short-channel DMOS structures.

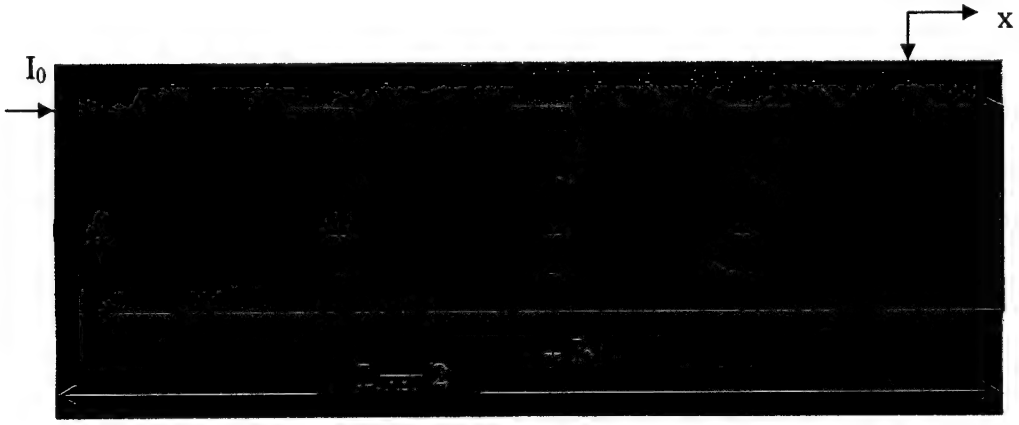
Figure 8.13 is used to model the accumulation channel resistance of the DMOS structure. Here, the current spreads from the channel to the JFET region through the accumulation layer. The sheet resistivity ρ_s is assumed to be uniform everywhere in the channel. The current through the accumulation channel has a 2D- nature, as it changes direction from lateral to vertical when flowing from the channel to the JFET region (see Fig. 8.13a). To model the conversion of current flow from lateral to vertical, the current in the accumulation channel is assumed to have a linear distribution [43], [69] (see Fig. 8.13c), and the equivalent circuit model is shown in Fig 8.13b. The current in the accumulation channel is given by

$$I(x) = I_0\left(1 - \frac{2x}{L_{JFET}}\right) \tag{8.3}$$

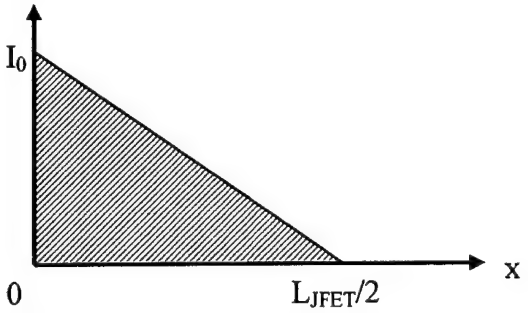
where I_0 is the total current at x=0. For an incremental distance dx, the power loss dP due to a transverse current I(x) is given by equation 8.4.



a) Structure used to calculate the accumulation channel resistance.



b) Equivalent circuit to model the current flow in the accumulation channel.



c) Current distribution in the accumulation layer.

Fig.8.13. Model of the DMOS structure to calculate the accumulation channel resistance.

$$dP = I(x)^2 \frac{\rho_s dx}{W} = I_0^2 \left(1 - \frac{4x}{L_{JFET}} + \frac{4x^2}{L_{JFET}^2}\right) \frac{\rho_s dx}{W} \tag{8.4}$$

The total power loss P is found by integrating equation (8.4) with respect to x from 0 to $L_{JFET}/2$ as follows:

$$P = \int_0^{L_{JFET}/2} dP = I_0^2 \frac{\rho_s L_{JFET}/2}{3W} = I_0^2 R_{accu} \tag{8.5}$$

The accumulation channel specific on-resistance is then given as

$$R_{accu,sp} = \frac{(L_{JFET}/2)S}{3\mu_{accu} C_{ox} (V_G - V_{TD})} \tag{8.6}$$

where L_{JFET} is the JFET length, S is the cell pitch, μ_{acc} is the accumulation channel mobility, C_{ox} is the oxide capacitance per unit area, V_G is the applied gate voltage, and V_{TD} is the threshold voltage of the accumulation channel. Sun et al. [49] demonstrated that at high gate voltages, the accumulation layer mobility decreases and is influenced by the fixed oxide charges and interface state densities in the same way as the inversion layer mobility. At low gate voltages, the accumulation layer mobility increases due to carrier screening and due to the spatial distribution of the majority carriers away from the surface. This is also seen from the effective mobility vs. gate voltage plot (see Fig. 6.2d) for the accumulation channel MOSFET by Cree [47], where the mobility peaks at 190 cm^2/vsec at low gate voltages, and drops to 30 cm^2/Vsec at a gate voltage of 20V. For simplicity, here we will assume the same mobility value for the inversion and accumulation layers. The threshold voltage of the accumulation channel depends on the doping of the n^- drift layer and is assumed to be $V_{TD}=V_{FB}$. The flatband voltage is then extracted from a C-V measurement on the n^- MOS capacitors.

Analyzing the results, we find that the source specific on-resistance is also a dominant component to the total $R_{on,sp}$. With the DMOSFET scaling, any misalignment

during the source and base contact formation increases the source specific on-resistance drastically. This also influences the accumulation channel and inversion channel resistances. The following examples will show that the overall $R_{on,sp}$ is very sensitive to the source specific on-resistance.

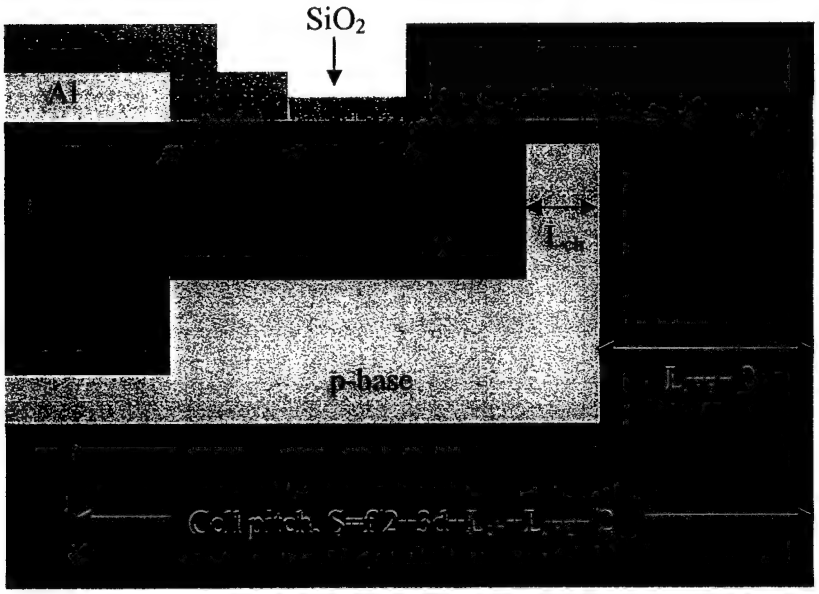


Fig. 8.14. Structure used for modeling the specific on-resistance of the DMOSFETs.

Case#1: An ideal case, where we have perfect alignments of the source and base contacts, as shown in Fig. 8.14. The source specific on-resistance is calculated from equation (8.6)

$$R_{source,sp} = \left(\rho_s L_{sn+} + \frac{\rho_c}{L_{cn+}} \right) S \qquad (8.6)$$

where L_{sn+}=2d is the length of the source region, S is the cell pitch, and L_{cn+}=d is the contact metal (Ni) and n^+ source overlap length. For 2-3 design rules, the alignment tolerance 'd' is 2 μm and the feature size 'f' is 3 μm, and for 3-5 design rules, d=3 μm

and f=5 μm. Here the transfer length L_T is replaced by L_{cn+}, as from the TLM measurements we find that $L_T=\sqrt{(\rho_c/\rho_s)}\approx 7.9\mu m$, and therefore the contact area to be used is $A_c=L_{cn+}W$. A sheet resistivity of $\rho_s=2.04\times10^3$ Ω/□ and a contact resistivity of $\rho_c=8.2\times10^{-4}$ Ω-cm^2 were used. The JFET and drift region resistances were then calculated by using equations 5.5, 5.9 through 5.11, with a doping of $3.2\cdot10^{15}$ cm^{-3} for the 4H-20 μm sample. The inversion channel specific on-resistance was calculated by using equation 5.1. An inversion threshold voltage of 6V was used in the calculations. The inversion and accumulation channel mobility of 15 cm^2/Vsec at a gate voltage V_G=20V was used. The accumulation channel specific on-resistance was calculated from equation 8.6. C-V measurements on a n$^-$ MOS capacitor gave a VFB=V_{TD}= -1.4V. Figure 8.15 shows the specific on-resistances vs. JFET length plot for the ideal case, where we have perfect alignments. From the plot we find that for small JFET length the drift and source resistance dominate. The accumulation channel resistance is small for small JFET gap. As the JFET gap increases, the JFET and drift region resistances decrease, but the source and accumulation channel resistances increase. At L_{JFET}=8 μm, the channel specific on-resistance is only (3.5mΩ-cm^2) 17% and the source specific on-resistance is (5.9 mΩ-cm^2) 29% of the total $R_{on,sp}$. $R_{source,sp}$ and $R_{accu,sp}$ are the dominant components and are each about (6 mΩ-cm^2) 30% of the total $R_{on,sp}$. With the $R_{ch,sp}$ scaled down, the $R_{source,sp}$ and $R_{accu,sp}$ become the dominant components of the specific on-resistance. By lowering the sheet resistance and improving the contact resistivity, we can lower the $R_{source,sp}$. By increasing the accumulation channel mobility or making V_{TD} more negative the $R_{accu,sp}$ can be lowered.

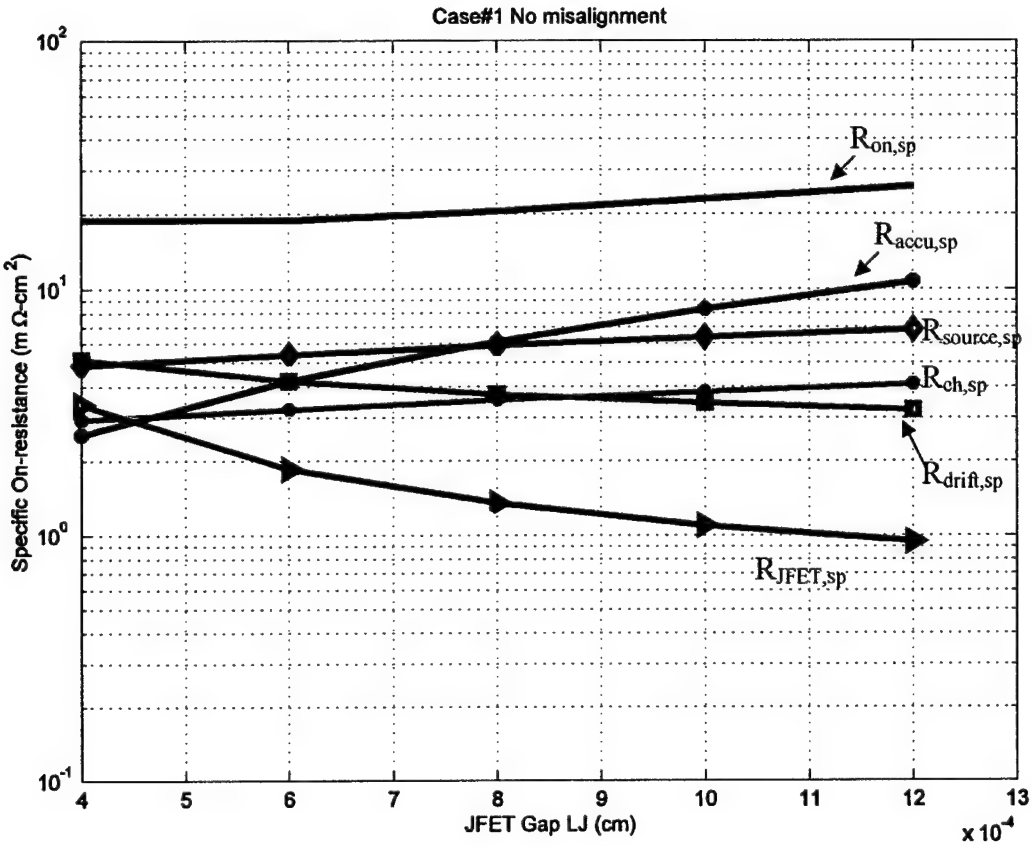


Fig. 8.15. Specific on-resistance versus JFET gap for the 4H-20μm sample with 2-3 design rules, and with no contact misalignment.

Case#2: We have seen from case#1 that even with perfect alignment the source resistance may be the dominant resistance. However, any misalignment of the masks that form the source can increase $R_{source,sp}$ even further. In this case, we assume 1 μm misalignment of the Ni contacts as shown in Fig. 8.16. The left side of the complete cell (see Fig. 8.16b) has a larger contact resistance than the right side of the cell. This will cause two different current flows through the inversion and accumulation channels. The point at which the two different current flow paths meet is moved from the cell center to a point X_m as shown in Fig. 8.16b. Assuming the y-directed current in the JFET region is uniform with repect to x, the current distributions in the accumulation layers are given by equation 8.7a and 8.7b.

$$I(x) = I_1\left(1 - \frac{x}{X_m}\right) \qquad 0 \le x \le X_m \tag{8.7a}$$

$$I(x) = I_1\left(\frac{x - X_m}{X_m}\right) \qquad X_m \le x \le L_{JFET} \tag{8.7b}$$

The ratio of currents at x=0 and at $x=L_{JFET}$ is then given by equation 8.8.

$$\frac{I_1}{I_2} = \frac{R_{s2} + R_{ch} + R_{accu2}}{R_{s1} + R_{ch} + R_{accu1}} = \frac{X_m}{L_{JFET} - X_m} \tag{8.8}$$

Solving for X_m using equation (8.6) for R_{accu},

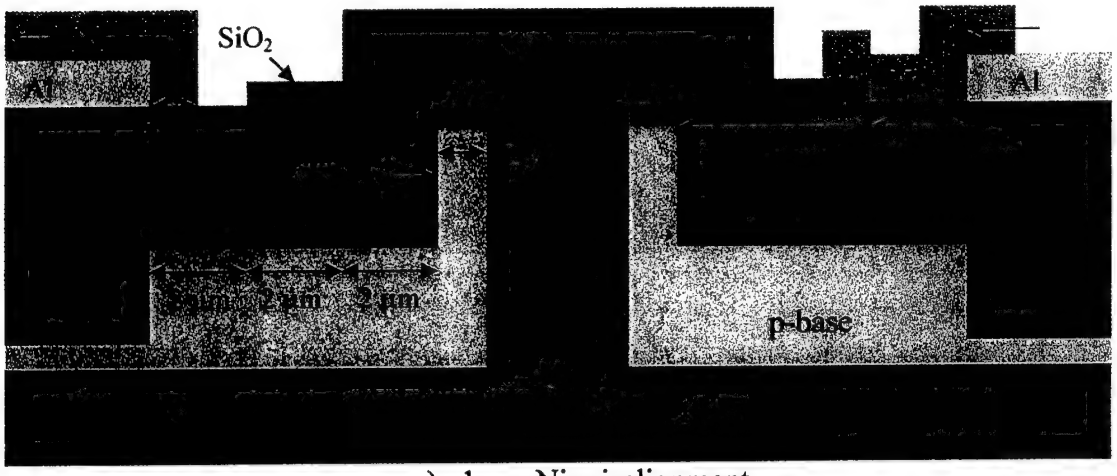
$$X_m = \frac{L_{JFET}}{2}\left[\frac{R_{s2} + R_{ch} + \dfrac{L_{JFET}}{3\mu_{accu}C_{ox}(V_G - V_{TD})W}}{\dfrac{(R_{s1} + R_{s2})}{2} + R_{ch} + \dfrac{L_{JFET}}{3\mu_{accu}C_{ox}(V_G - V_{TD})W}}\right] \tag{8.9}$$

Special cases are: $R_{s1}=R_{s2}$ $X_m=L_{JFET}/2$

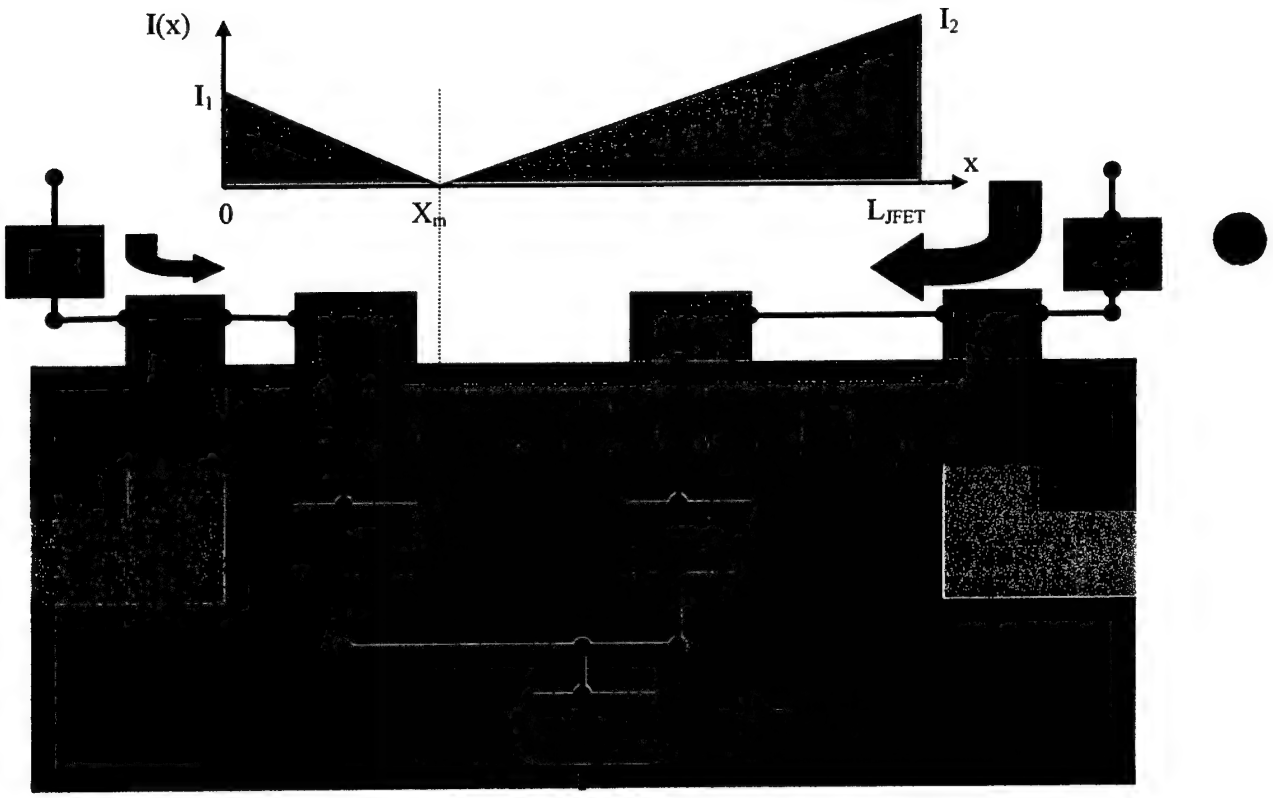
$R_{s1} \rightarrow \infty$ $X_m=0$

$R_{s2} \rightarrow \infty$ $X_m=L_{JFET}$

Knowing X_m, the overall specific on-resistance $R_{on,sp}$ due to the 1 μm Ni misalignment can be calculated. The resulting specific on-resistances as a function of the JFET length are then plotted in Fig. 8.17. The total resistance $R_{ch,sp}+R_{JFET,sp}+R_{accu,sp}$ is 89% of the $R_{on,sp}$ for a JFET length of 8 μm. Figure 8.17 also shows some measured data (circles) for the 4H-20μm sample with 2-3 design rules. The lines represent the resistances calculated from the spreadsheet. A threshold voltage V_T=6.0V and V_{TD}=-1.4V, effective channel mobility of $\mu_{ch}=\mu_{accu}$=15 $cm^2/Vsec$, sheet resistivity of $\rho_s=2\cdot10^3$ Ω/□, and a contact resistivity of $\rho_c=8.2\cdot10^{-4}$ Ω-cm^2 were used.



a) 1 μm Ni misalignment



b) Current distribution in the accumulation layer.

Fig. 8.16. Structure used to calculate the specific on-resistances of the DMOS structure assuming 1 μm Ni misalignment.

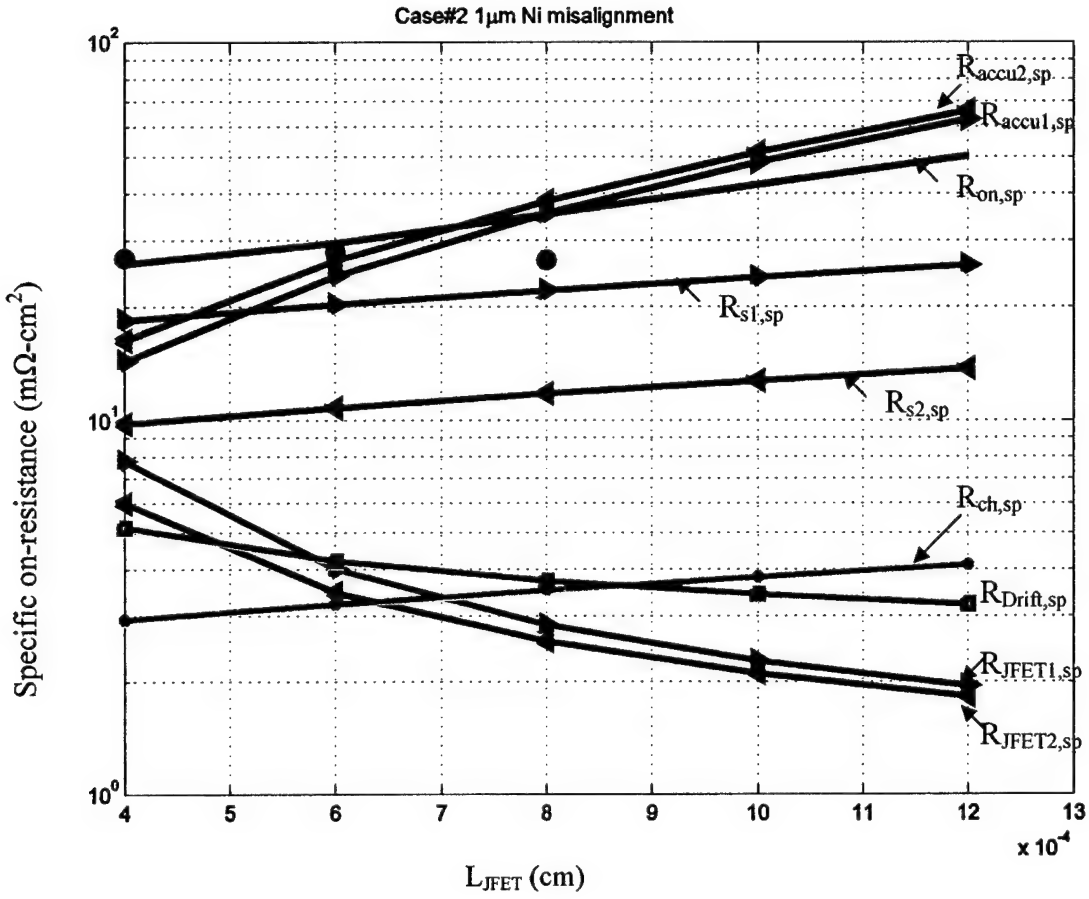
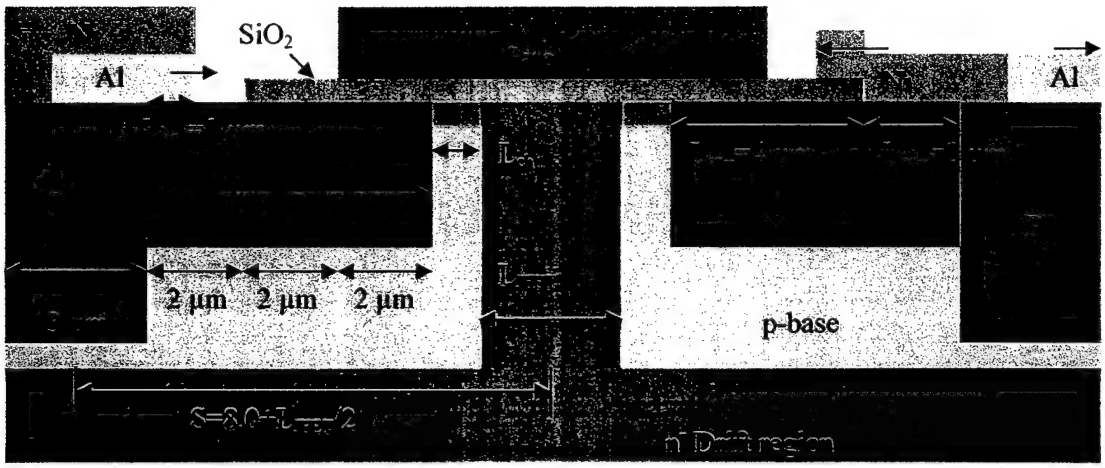


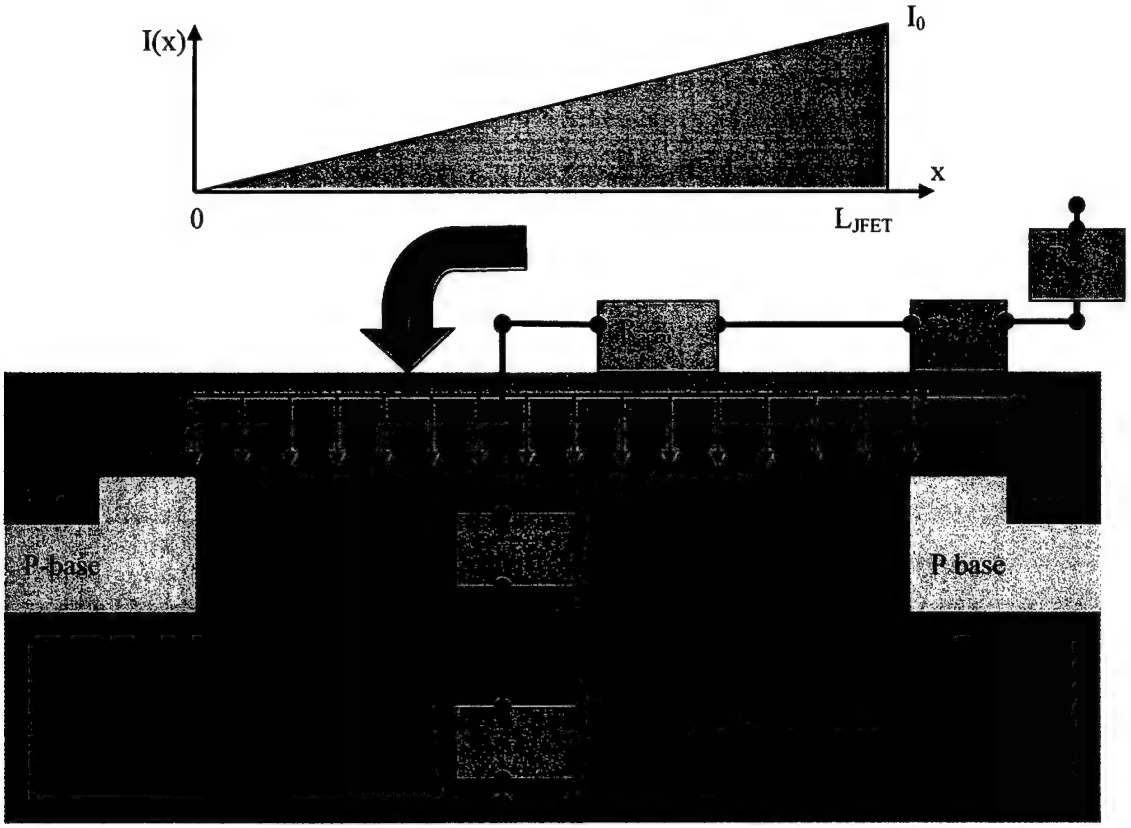
Fig. 8.17. Specific on-resistance of the 0.5 μm channel length DMOSFETs on the 4H-20μm sample for 2-3 design rules, assuming 1μm misalignment of the Ni contacts. The circles are the measured data and the solid lines are the specific on-resistances from the spreadsheet calculations.

Case#3: In this case, we assume 1 μm misalignment of the Ni source contact and 1 μm misalignment of the Al base contact, as shown in Fig. 8.18. Here, on one side of the complete cell we loose contact to the source completely, and on the other side of the cell we have an ideal contact to the source. The average source resistance is then calculated for the complete cell, and the resulting specific on-resistances are $R_{source,sp}=2xR_{source,sp}$ (Case#1), $R_{ch,sp}=2xR_{ch,sp}$(Case#1), and $R_{accu,sp}=4xR_{accu,sp}$(Case#1). Figure 8.19 shows the specific on-resistances vs. JFET length with 1 μm misalignment of the Ni contact and 1 μm misalignment of the Al base contact. The accumulation channel resistance dominates, and is 47% of the total $R_{on,sp}$ for $L_{JFET}=8\mu m$. The inversion channel resistance is only 14% and the source resistance is 27% of the total $R_{on,sp}$. As the DMOS structure is scaled down, any misalignment can significantly increase the overall specific on-resistance.

Figure 8.20 shows $R_{on,sp}$ vs. gate voltage for a device (m2163) with 2-3 design rules and with a JFET length of 8 μm. The specific on-resistances were extracted from the I_d-V_{ds} plots at different gate voltages. The device has a threshold voltage of $V_T=5.8V$, extracted from the I_d-V_{gs} plot at $V_{ds}=0.4V$. The measured oxide thickness is 425^0A. From the plot we see that the specific on-resistance increases as the gate voltage is decreased. This indicates that the channel (inversion plus accumulation) specific on-resistance is dominating. For a $3.2\cdot10^{15}$ cm^{-3} doping and 20 μm epilayer thickness, the drift specific on-resistance and the JFET specific on-resistances are 3.72 mΩ-cm^2 and 1.35 mΩ-cm^2 respectively. Figure 8.20a also shows a fit to the measured data. The fitting parameters extracted were $V_T=5.67V$, effective channel mobility $\mu_{ch}=10$ $cm^2/Vsec$, and $C=R_{Drift,sp}+R_{JFET,sp}+R_{source,sp}=21.8$ mΩ-cm^2. C components are independent of the applied gate voltage. The inversion and accumulation channel resistances are the only voltage dependant components, and increases as the gate voltage is decreased. Table 8.1 shows the summary of results from the plot.



a) 1 µm Ni misalignment and 1 µm Al misalignment



b) Current distribution in the accumulation layer.

Fig. 8.18. Structure used to calculate the specific on-resistances of the DMOS structure assuming 1 µm Ni misalignment and 1µm Al misalignment.

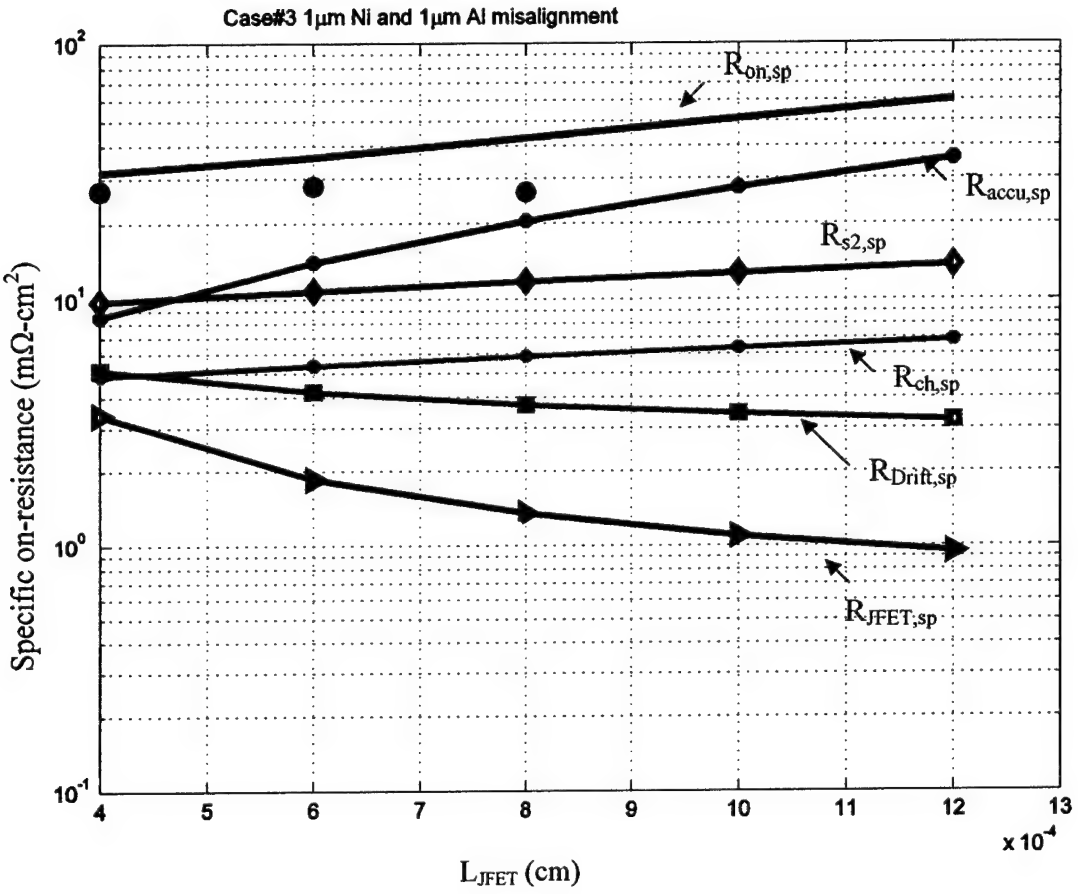
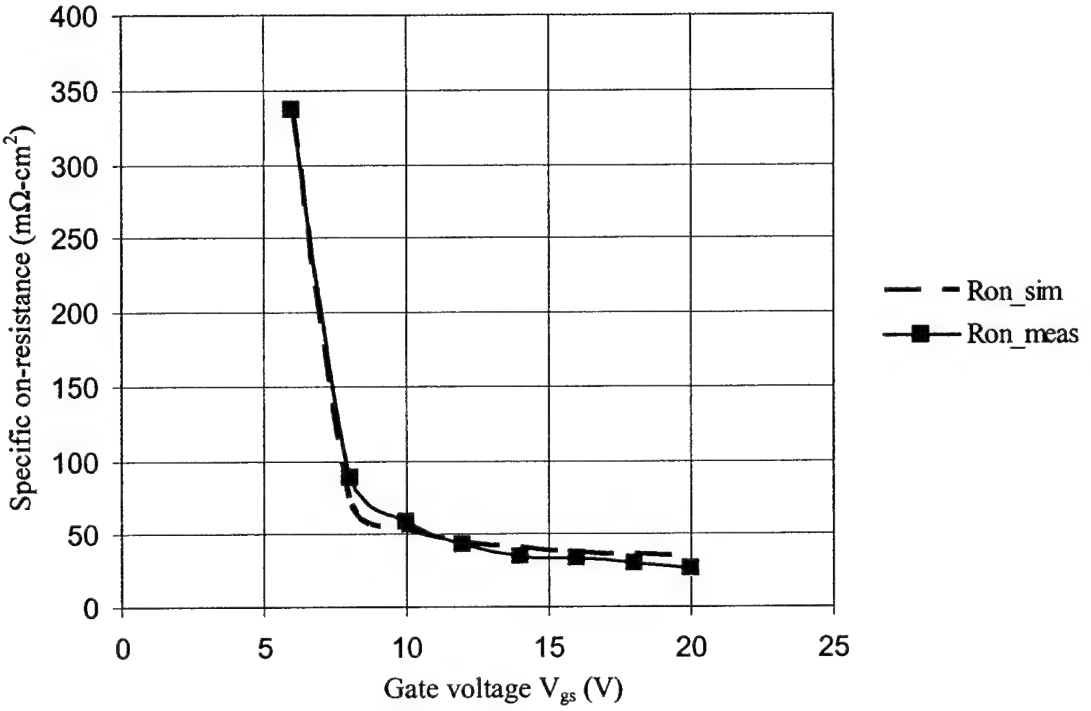
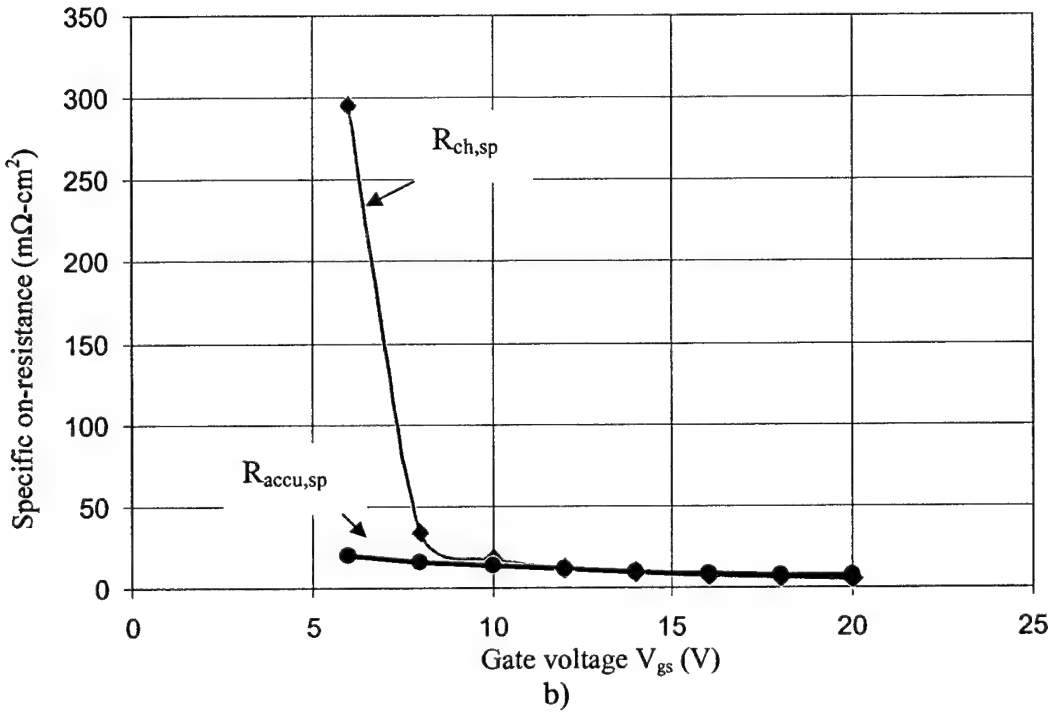


Fig.8.19. Specific on-resistance of the 0.5 μm channel length DMOSFETs on the 4H-20μm sample for 2-3 design rules, assuming 1μm misalignment of the Ni contacts and 1μm misalignment of the Al contacts . The circles are the measured data and the solid lines are the specific on-resistances from spreadsheet calculations.



a)



b)

Fig. 8.20. Specific on-resistance as a function of the applied gate voltage for a device (m2163) on the 4H-20μm sample, with 2-3 design rules.

Table 8.1

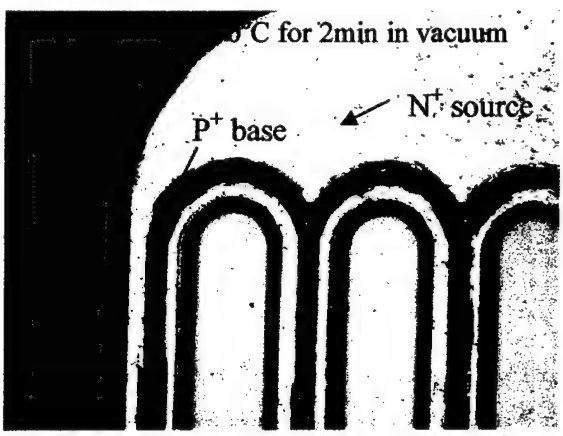
Gate voltage V_g (V)	$R_{on,sp}$ (mΩ-cm^2) (Measured)	$R_{on,sp}$ (mΩ-cm^2) (Simulated)	$R_{ch,sp}$ (mΩ-cm^2) (Simulated)	$R_{accu,sp}$ (mΩ-cm^2) (Simualted)
6	336.2	336.4	294.5	20.0
8	89.1	70.4	32.8	15.8
10	58.5	52.2	17.4	13.0
12	43.1	44.7	11.8	11.1
14	34.5	40.4	9.0	9.6
16	33.0	37.6	7.2	8.6
18	30.3	35.5	6.0	7.6
20	26.6	34.0	5.2	7.0

From the table and Fig. 8.20b we find that at high gate voltages the accumulation resistance is larger than the inversion channel resistance. As the gate voltage is decreased and close to the threshold, the channel resistance increases rapidly to turn the device off. At a gate voltage of 20V, the source specific on-resistance dominates and is 49% of the total $R_{on,sp}$. The inversion channel resistance only 15% and the accumulation channel resistance is 20% of the overall specific-on resistance. With the accumulation resistance included in the model, we can now account for the large difference between the measured $R_{on,sp}$ values and the values calculated in Chapter 5, where the accumulation resistance was neglected. The values in Table 8.1 indicate that in the full-on condition (V_g=20V), the specific on-resistance of the MOSFET channel is no longer the dominant component of the on-resistance. This is in marked contrast to the other "long channel" DMOSFETs, where the channel resistance typically dominate the on-resistance of the device, even at the highest allowable gate voltages.

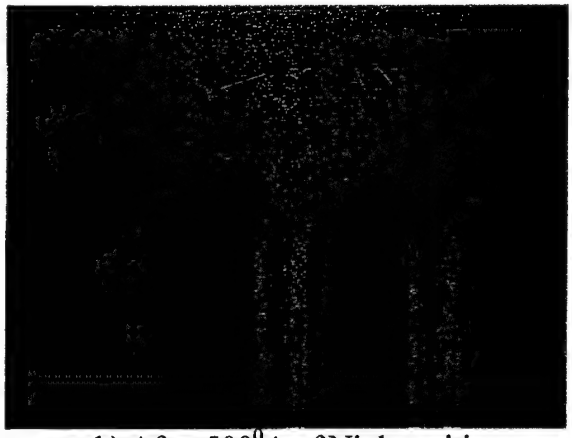
8.4 Contact Anneal Experiment

In order to improve the contact resistivity of the 4H-20 μm sample, the top metal (Au) was removed and 500^0A of Ni was re-deposited by e-beam evaporation. The sample was then re-annealed at 950^0C for 2 minutes in vacuum. During the contact anneal process, the temperature inside the chamber got hotter than 1453^0C (melting point of Ni), as later when inspected under an optical microscope, we found the Ni on the source region melted and shorted to the gate fingers. The melting point of silicon is 1410^0C and the polysilicon gates also looked damaged after the contact anneal. We suspect that the thermocouple was not properly attached to the susceptor by thermal paste, and the heater controller tried to drive the heater to a higher temperature in order to reach to the set temperature. Figures 8.21a, b and c show 4H-20μm sample before and after the 950^0C contact anneal step.

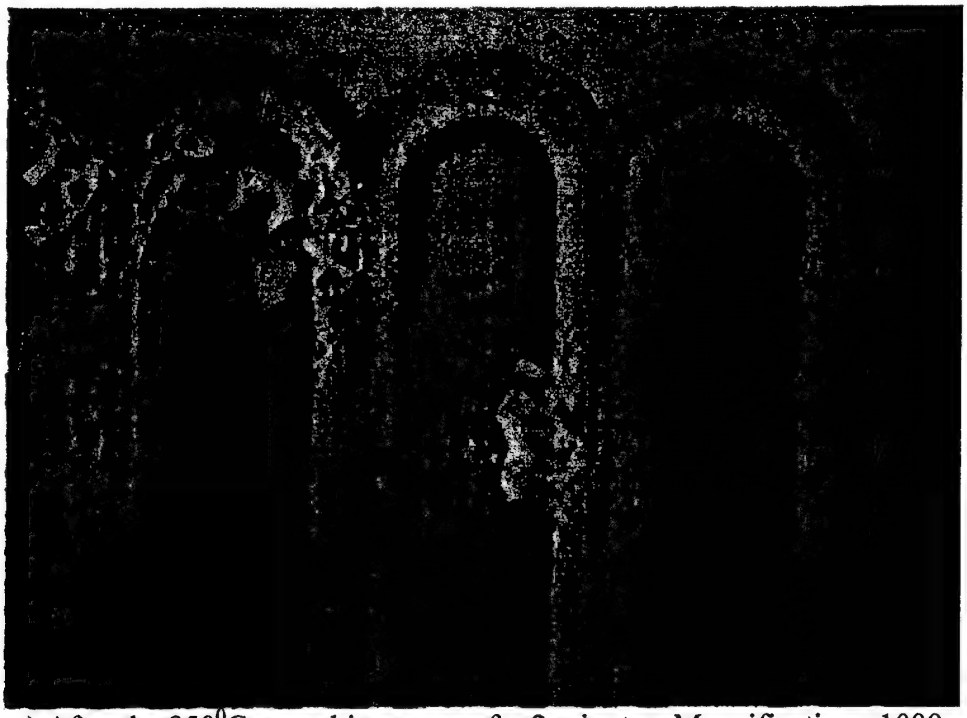
Before annealing the 4H-50μm sample, a new thermocouple was attached to a new susceptor with thermal paste. A test run was then performed by annealing a 6H-SiC test sample with (500^0A) Ni and (700^0A/500^0A) Ni/Al contact metals. The sample was placed on a Si-wafer in order to avoid any contaminations from the susceptor. The test piece was annealed at 900^0C for 2 minutes in 400mT Ar pressure in order to avoid any Al evaporation. Figures 8.22a and b show optical photographs before and after the contact anneal. The Ni contacts did not look very shiny, and inspection under SEM revealed that after the contact anneal, Ni has formed into small balls. Figures 8.22c and d show the SEM photographs of the test sample. The 4H-50 μm sample was then annealed at 900^0C in 400mT Ar for 2 minutes.



a) After top metal (Au) removal. Magnification x1000.



b) After 500^{0}A of Ni deposition. Magnification x1000.

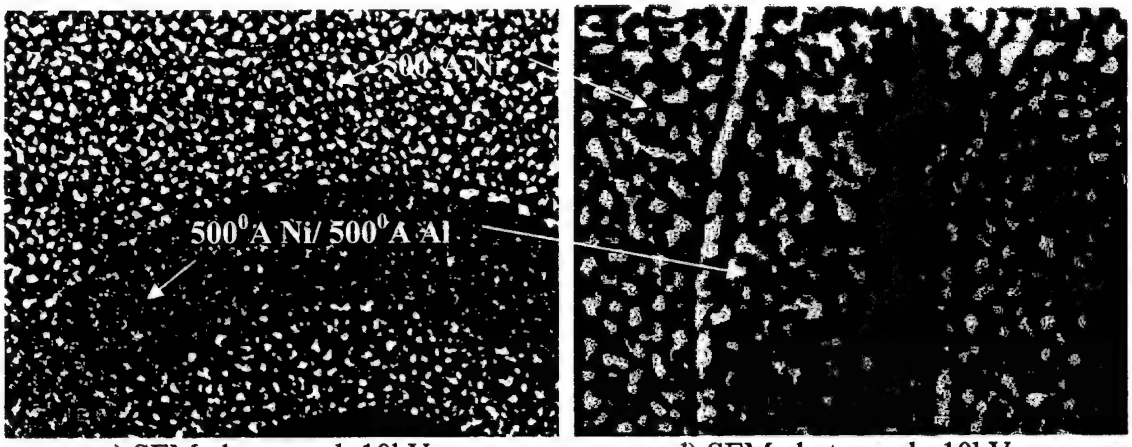


c) After the 950^{0}C anneal in vacuum for 2 minutes. Magnification x1000.

Fig. 8.21. 4H-20μm sample before and after the 950^{0}C contact anneal (second anneal).

a) Test sample before contact anneal.
Magnification x1000

b) Test sample after contact anneal.
Magnification x1000



c) SEM photograph,10kV.
Magnification x5000.

d) SEM photograph, 10kV.
Magnification x9500.

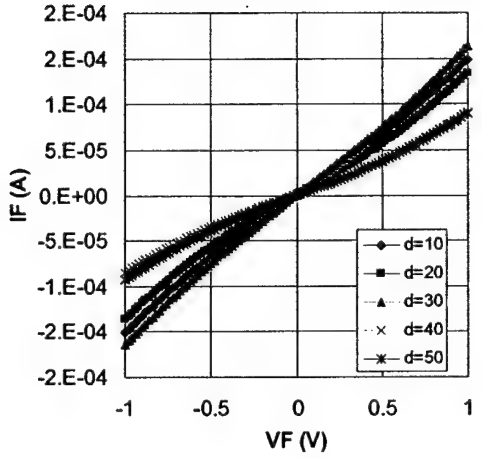
Fig. 8.22. Contact anneal experiment performed on 6H-SiC test piece before annealing the 4H-50μm sample at 900^{0}C in 400mT Ar pressure for 2 minutes.

8.5 Device Performance during the On- and Off-State of the 4H-50μm Sample

After the 900^0C contact anneal on the 4H-50μm sample, 3500^0A of Au top metal was deposited by e-beam evaporation. The Ni in the source region looked dark in most of the devices, except one or two places it looked very shiny. The TLM data on the dark colored n^+ TLM structures were random and showed non-linear I-V characteristics. As shown in Figure 8.23 the sheet resistance measured was $2.2 \cdot 10^4 \Omega/\square$ and contact resistance was $3.5 \cdot 10^{-2} \Omega\text{-cm}^2$. However, TLM measurements on the shiny Ni contacts, gave a contact resistance of $3.1 \cdot 10^{-5}$ $\Omega\text{-cm}^2$ and a sheet resistance of $2.1 \cdot 10^3 \Omega/\square$ as shown in Fig. 8.24. Figure 8.25 shows the TLM measurements on the p^+ base contact regions. The sheet resistance measured was $2.4 \cdot 10^4 \Omega/\square$ and the contact resistance was $2.1 \cdot 10^{-2}$ $\Omega\text{-cm}^2$. The Ni source contact areas on the DMOSFETs looked dark.

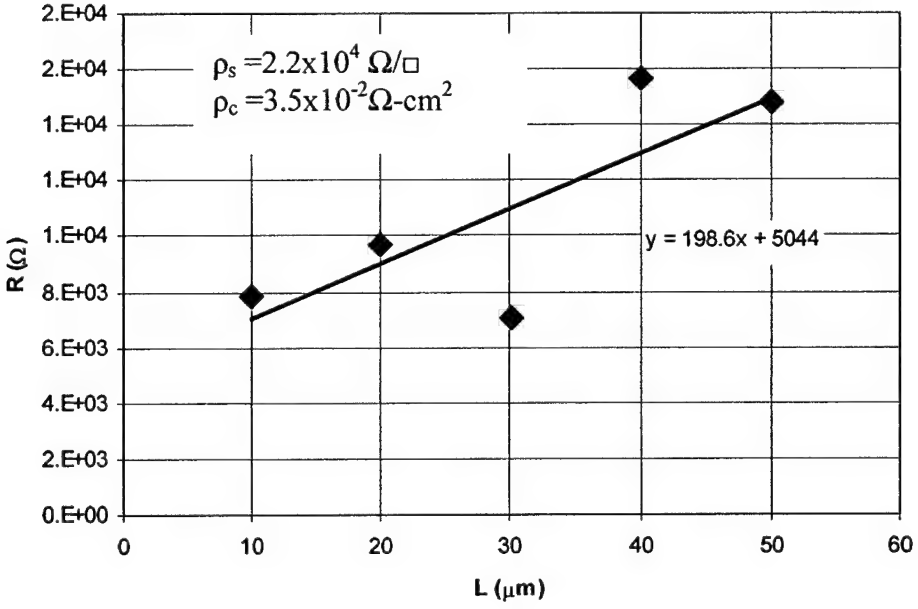
Figures 8.26a, b and c show the forward I-V characteristics of DMOSFETs on the 4H-50μm sample with L_{JFET} of 4, 6 and 8μm respectively. The specific on-resistance extracted were $117 m\Omega\text{-cm}^2$, $83.1 m\Omega\text{-cm}^2$, and 74.4 $m\Omega\text{-cm}^2$ respectively. The $R_{on,sp}$ increases with the increase in JFET resistance as we go from L_{JFET} of 8 μm to 4 μm. The on-resistance measured is higher than expected.

Figure 8.27 shows the fit of specific on-resistance from spread sheet calculations to the measured values obtained from short channel MOSFETs with 2-3 design rules on the 4H-50μm sample as a function of the JFET gap. The specific on-resistances were calculated from the spreadsheet assuming 1 μm Ni misalignment and 1 μm Al misalignment. A threshold voltage of 4.0V and a channel mobility of 15 cm^2/Vsec at a gate voltage of 18V were used. The doping and the thickness of the drift region were $9.0 \cdot 10^{14}$ cm^{-3} and 50 μm respectively. A sheet resistance of $2.2\text{x}10^3 \Omega/\square$ and contact resistance of $5\text{e-}3 \Omega\text{-cm}^2$ (shiny contacts) were used. However, the DMOSFET source contacts looked dark and the contact resistance may be higher. From the plot we find that the JFET resistance dominates for small JFET length and decreases rapidly for larger JFET length. For a L_{JFET}=8μm, the accumulation channel resistance is 42% of the total $R_{on,sp}$. The drift region is 25% and the JFET resistance is 17% of the total $R_{on,sp}$. The inversion channel is only 11% of the total $R_{on,sp}$. The red circles represent the measured



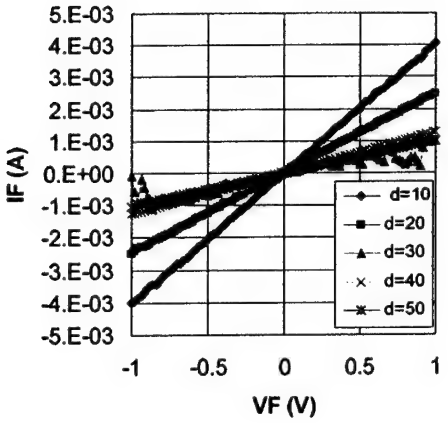
a) Non-linear I-V profiles of the TLM structures

b) n^+ TLM structures where Ni contacts looked dark. Magnification x200.

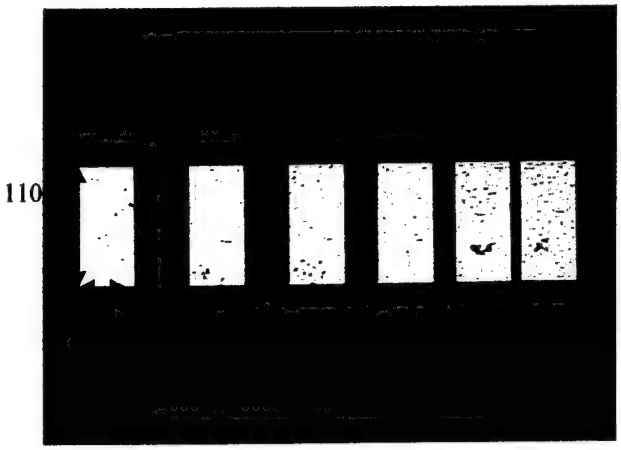


c) TLM data from the n^+ source region

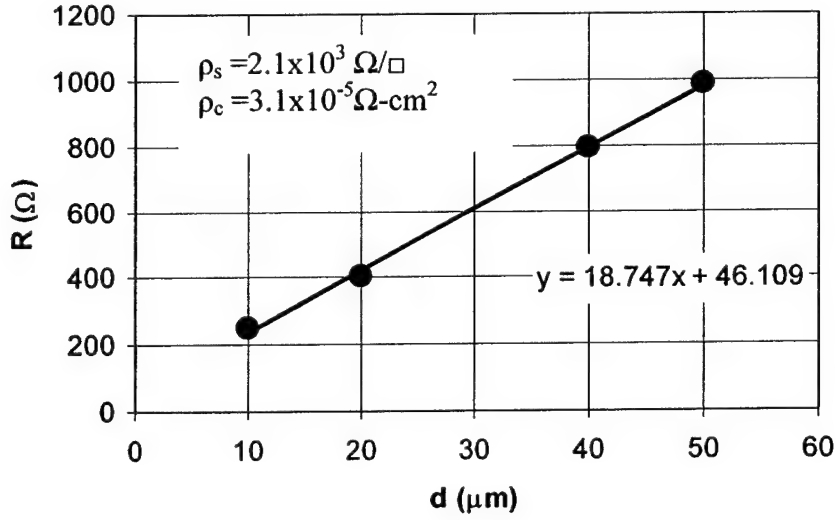
Fig. 8.23. TLM measurements of the contact resistivity and sheet resistance for the n+ source region on 4H-50μm sample where Ni contacts looked dark.



a) Linear I-V characteristics of the TLM structures.

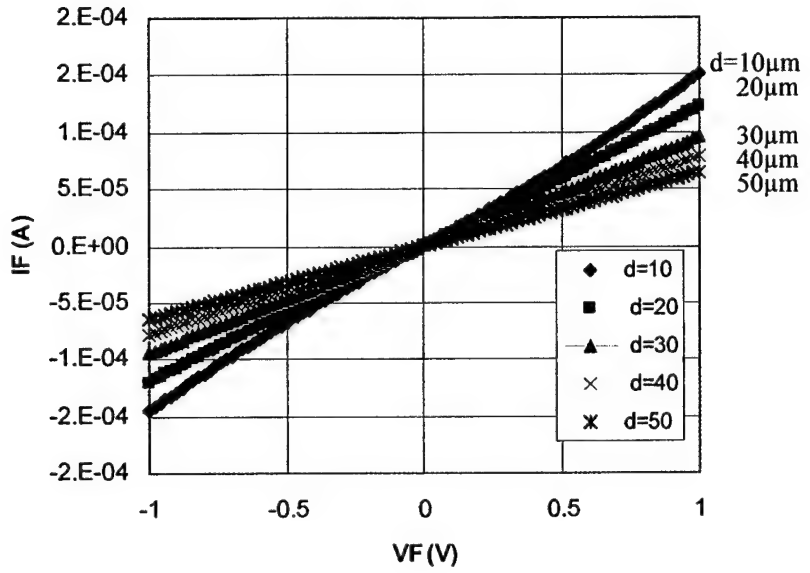


b) TLM structures where Ni looked shiny. Magnification x200.

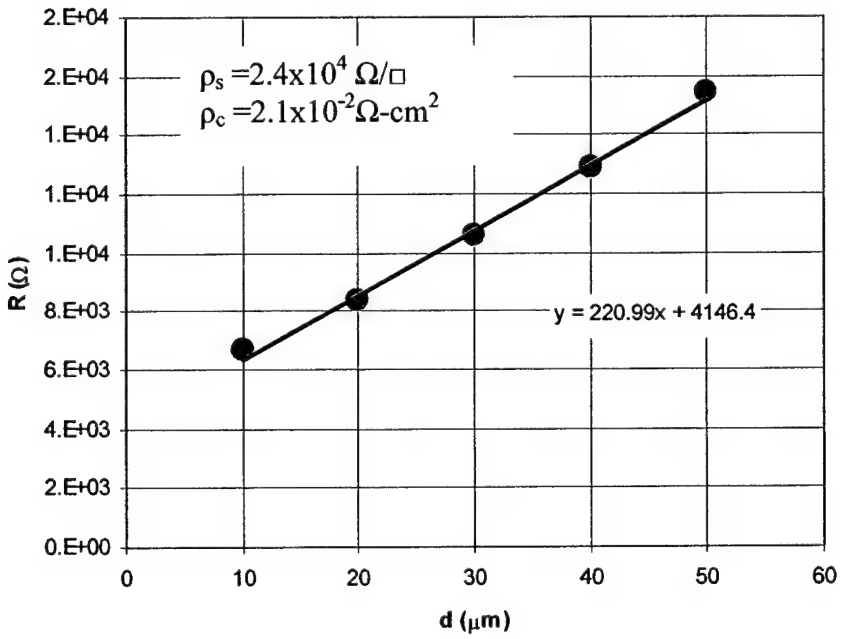


b) TLM data for the n^+ source region.

Fig. 8.24. TLM measurements of the contact resistivity and sheet resistance for the n-type source region on 4H-50μm sample where Ni contacts looked shiny.



a) I-V characteristics of the TLM structures in p^+ base region.



b) TLM data for the p^+ base region.

Fig. 8.25. TLM measurements of the contact resistivity and sheet resistance for the p-type base region on 4H-50µm sample.

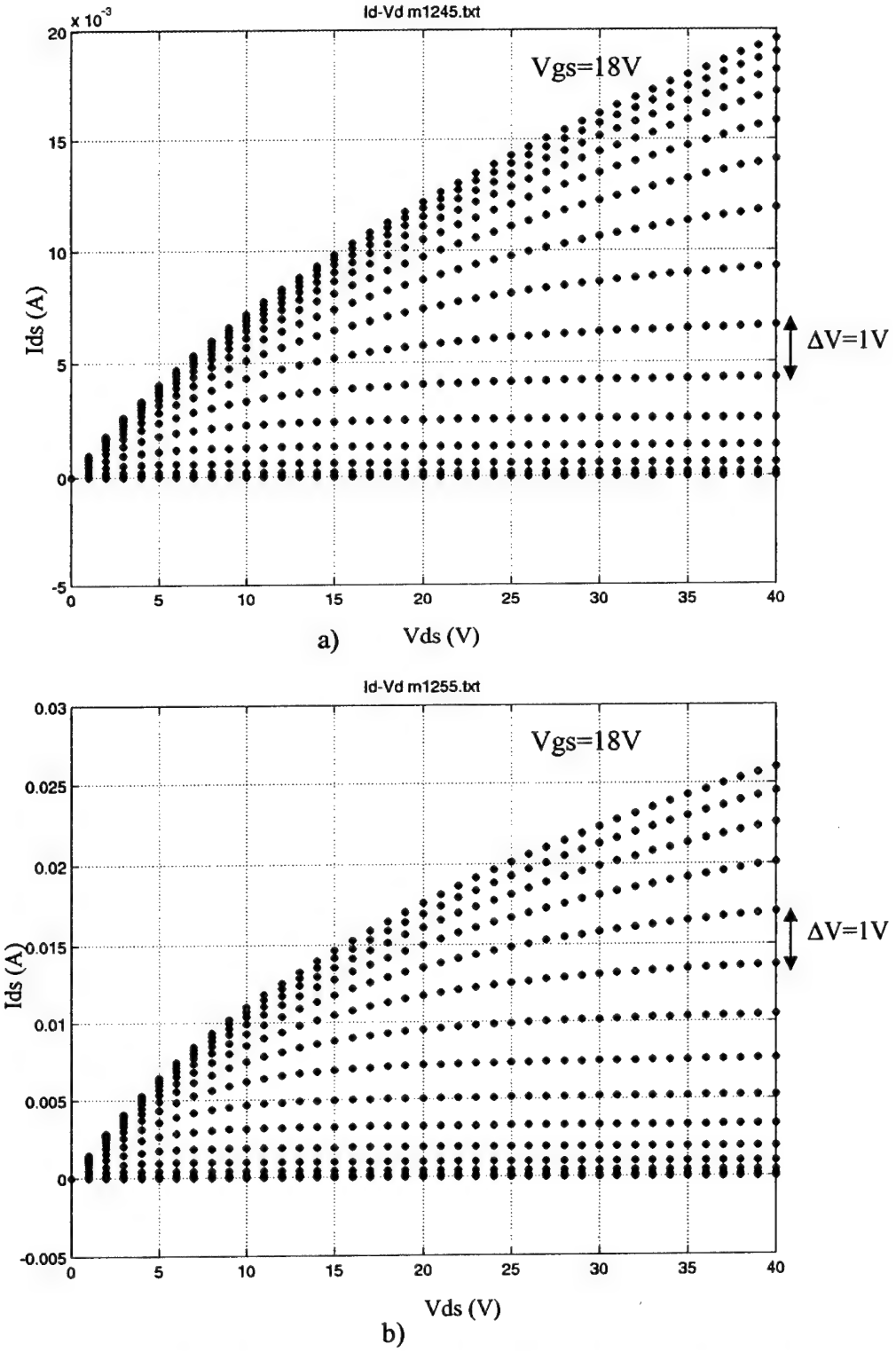


Fig. 8.26. a) I-V for DMOSFETs on the 4H-50μm with with 2-3 design rules, L_{JFET}=4μm, A=$1.04 \cdot 10^{-4}$ cm^2 and b) L_{JFET}=6μm, A=$1.144 \cdot 10^{-4}$ cm^2.

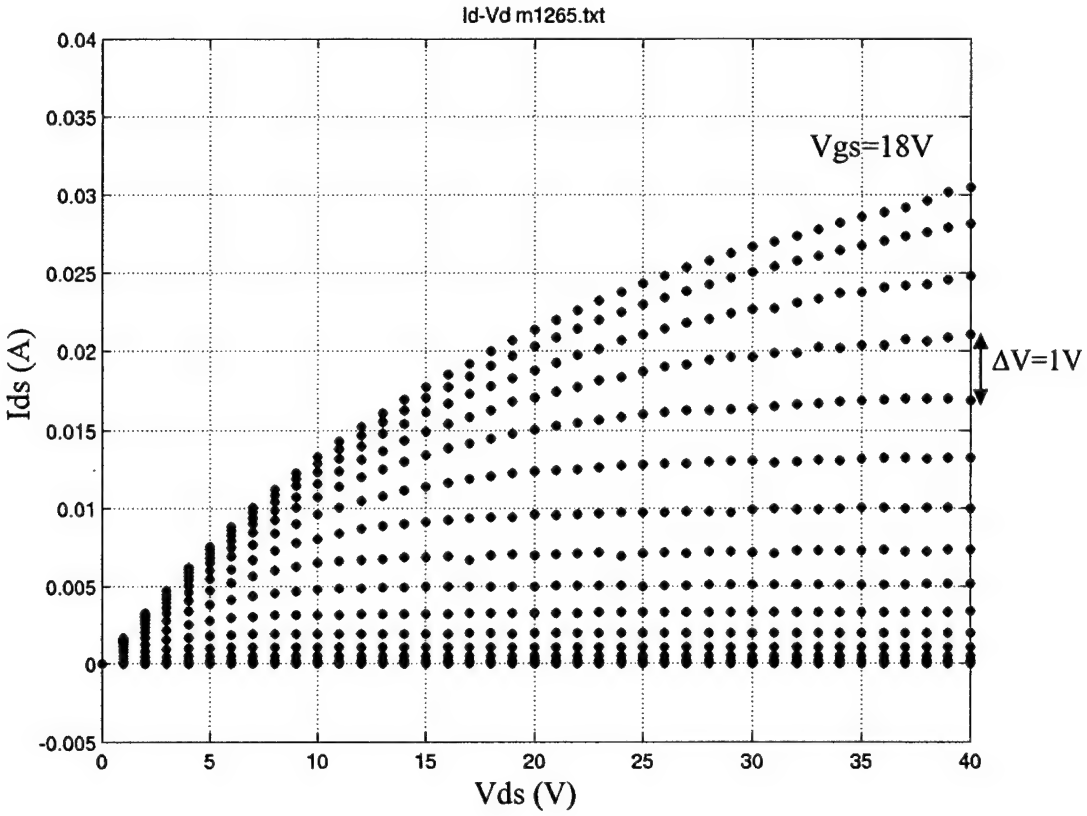


Fig. 8.26c. Forward drain characteristics of a DMOSFET on the 4H-50μm sample with 2-3 design rules, L_{JFET}=8μm and A=1.248·10^{-4} cm^{-2}.

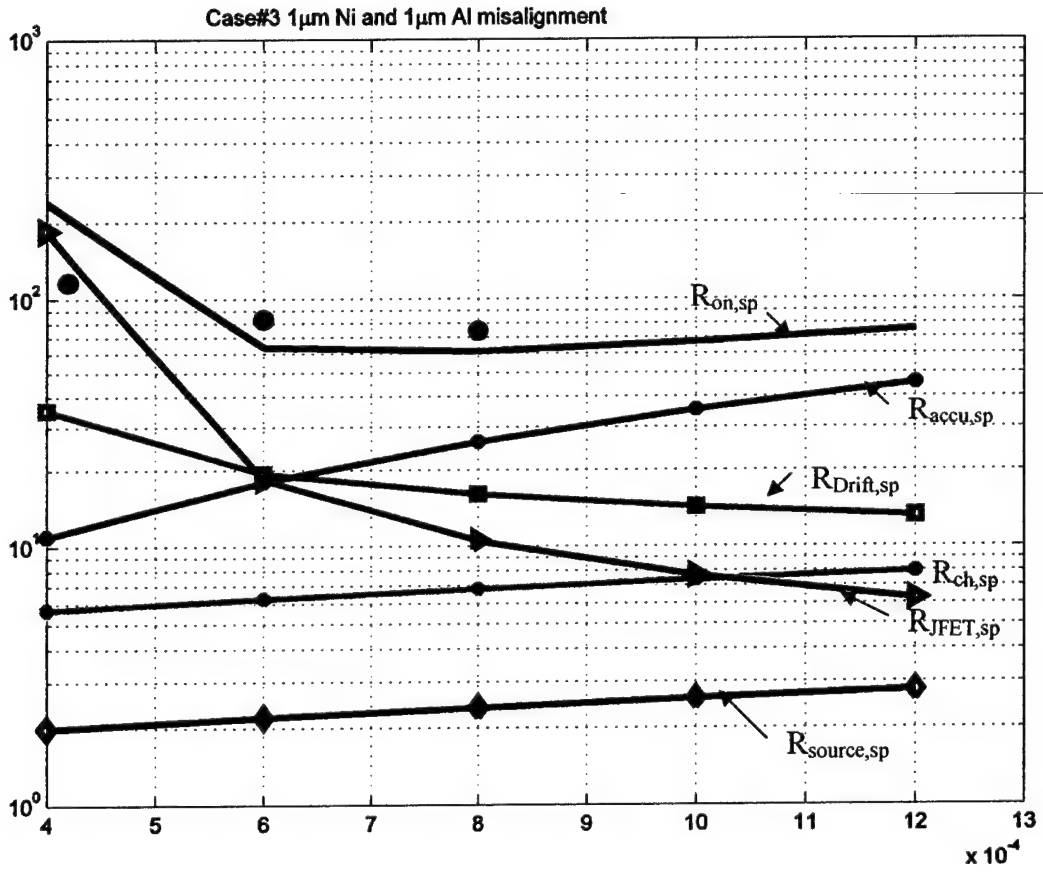


Fig.8.27. Specific on-resistance of the 0.5 μm channel length DMOSFETs on the 4H-50 μm sample for 2-3 design rules, assuming 1μm misalignment of both the Ni and Al contacts . The circles are the measured data and the solid lines are the specific on-resistances from the spreadsheet calculations.

data from the 4H-50μm sample with 2-3 design rules. The lines represent the series resistance calculated from the spreadsheet.

The off-state characteristics were obtained by grounding the source and gate and applying a positive voltage to the drain. Figure 8.28a shows the off-state characteristics of a DMOS structure on the 4H-50μm sample. The blocking voltage capability of the MOSFETs and diodes were drastically reduced after the implant contact anneal step. Figure 8.29 shows a distribution of the breakdown voltage versus the JTE width. The best JTE diodes blocked higher voltage than the best non-JTE diodes. Most of the tested diodes and MOSFETs were reaching the 1mA limit close to 2000V rather than catastrophically breaking down. This may be caused by aluminum spiking of the p^+ contacts after the 900^0C contact anneal. Figure 8.28b shows a photograph of a device which catastrophically broke down. In this case the JTE edge was visible, and a crater is located near the JTE edge, suggesting breakdown at the JTE edge.

Figure 8.29 shows a trend line of the highest breakdown voltage vs. JTE width. If we ignore the diodes with low breakdown voltage, assuming that isolated defects lower the blocking voltage, the trend in blocking voltage with JTE width is what we expect, except that the breakdown strength is too low. The theoretical breakdown voltage for a 50 μm epilayer is 6 to 7kV. No high voltage testing was performed prior to the contact anneal. However, high voltage measurements after the implant activation anneal showed a diode blocking 4.5kV with a JTE width of 150μm (see Fig. 7.25). This indicated that the JTE was working, and the reduction of blocking capability from 4.5kV to 2kV is probably process related. We can eliminate the gate oxide as a possible failure mechanism, as the diodes are showing the same blocking capability as the MOSFETs.

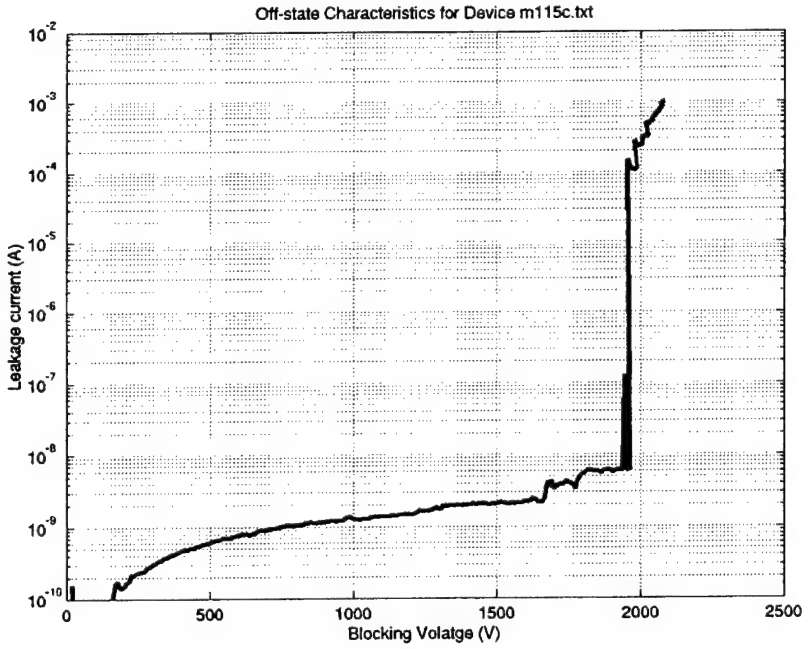


Fig. 8.28a Off-state characteristics of a DMOS structure on the 4H-50μm sample.

Fig. 8.28b Photograph of a short channel DMOSFET after catastrophic breakdown.

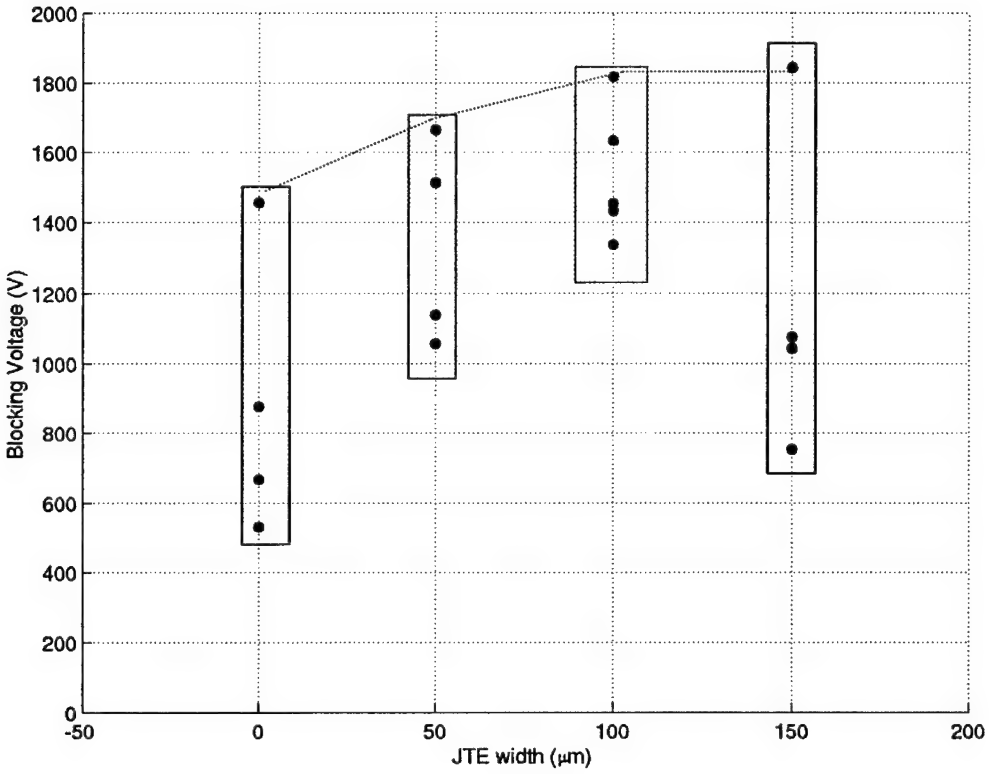
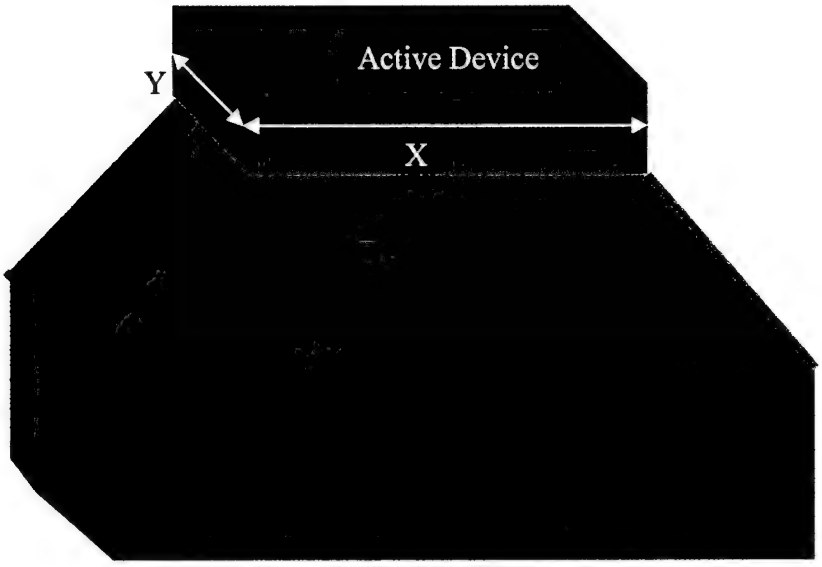


Fig. 8.29. Distribution of the blocking voltages with JTE width from diode measurements on the 4H-50μm sample.

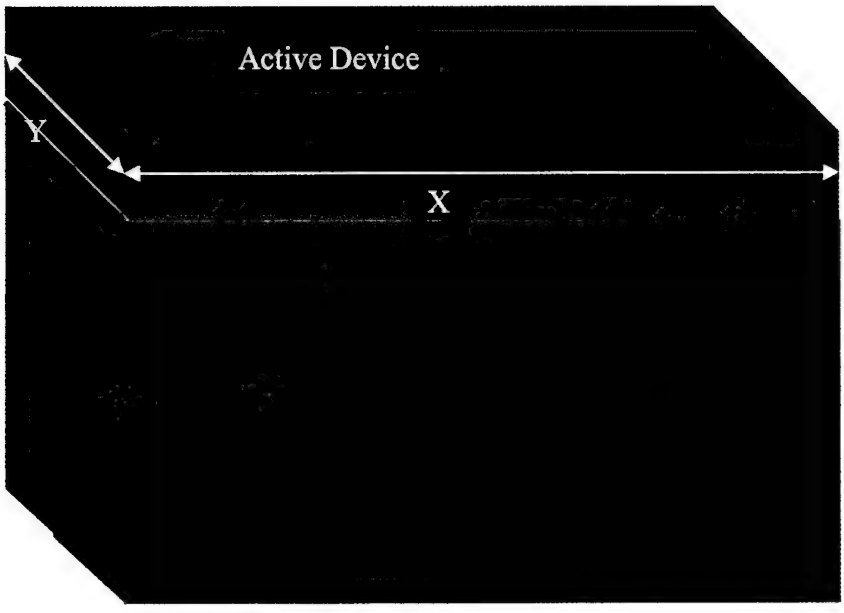
8.6 Correction of the Ron,sp for Small Area Devices

For the small area devices, where device dimensions are comparable to the drift region thickness, the specific on-resistance calculated from the linear region of the I-V characteristics multiplied by the device active area may give an artificially low value. This is due to the lateral current spreading in the drift region when current flows from the small active device through the drift layer and into the large drain contact. For large area devices, this effect is negligible and the measured $R_{on,sp}$ should be close to the true value.

In order to make corrections to the extracted $R_{on,sp}$, 3D device simulations were performed using Davinci [70]. Figures 8.30a and b show the structures used in the simulation for calculating the drift region resistance with and without current spreading respectively. The Davinci program solves Poisson's equation and both electron and hole current continuity equations to analyze device structures similar to the MEDICI program, the only difference is the 3D grid structures. The drift region resistances with and without current spreading were calculated for epilayer thickness of 20μm and a doping of $3.2 \cdot 10^{15}$ cm^3, and epilayer thickness of 50 μm with a doping of $9 \cdot 10^{14}$ cm^{-3}. A 250 μm thick drain contact with a doping of $6 \cdot 10^{18}$ cm^{-3} was also included. To model the spreading resistance ($R_{drift,sp,spreading}$) , the active area of the top contact was made much smaller than the drain contact and varied according to the 2-3 and 3-5 design rules. Figures 8.31 and 8.32 show the current spreading due to the small active area on the 4H-20μm and 4H-50μm samples respectively. The drift region resistance without spreading ($R_{drift,sp,wospreaing}$) was then modeled with large area contacts on both top and bottom of the drift layer. Figure 8.33 shows the current flow vectors for the structure without current spreading for the 4H-20μm sample.



a)



b)

Fig. 8.30. Structures used in 3D Davinci simulations. The top structure represents a small device with current spreading, and the bottom structure represents a large area device without any current spreading.

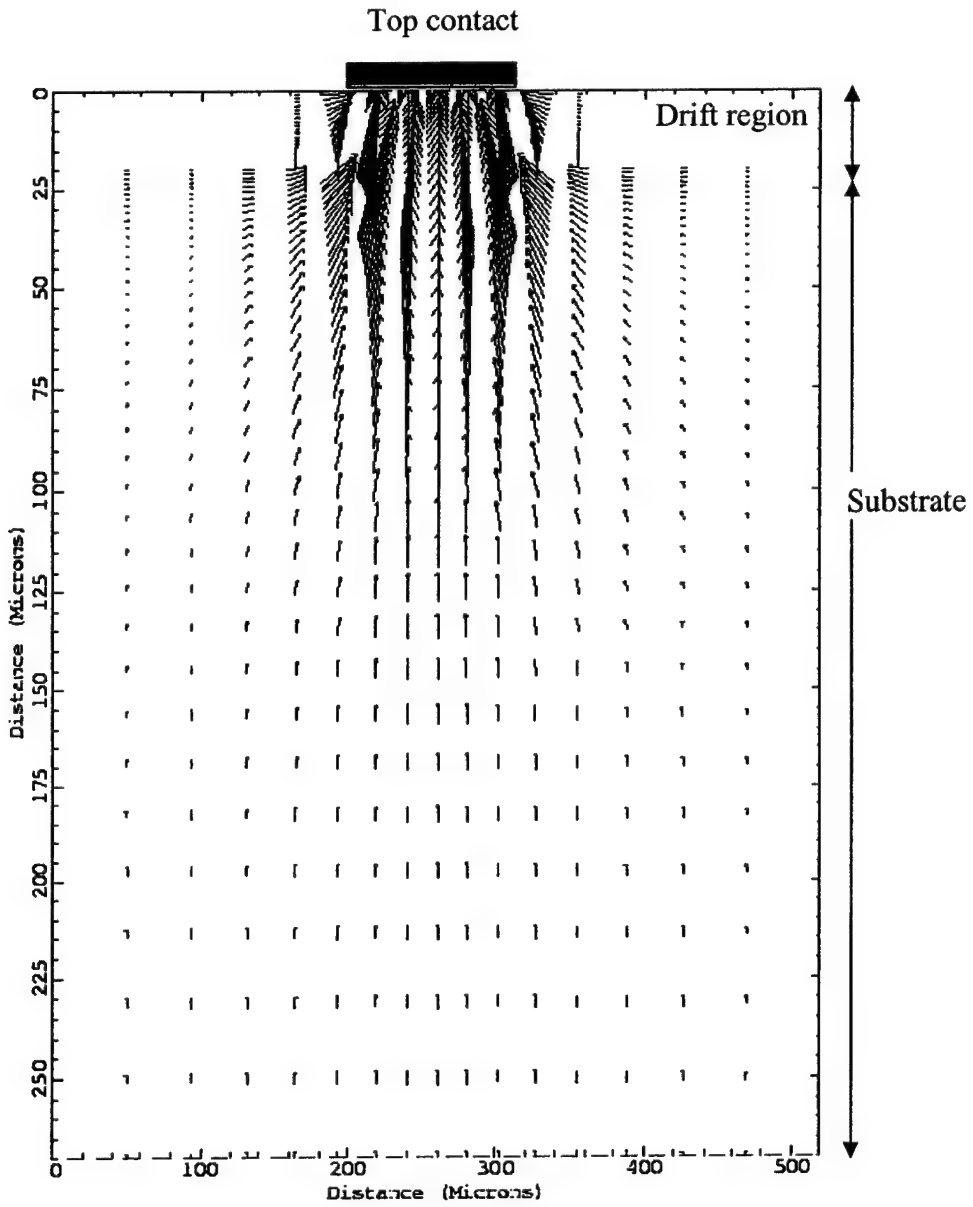


Fig. 8.31. Current flow vectors showing current spreading in the drift region. The top contact area equals to the area for a device with 2-3 design rules and L_{JFET}=8μm. The epilayer doping is $3.2 \cdot 10^{15}$ cm^{-3} and thickness is 20μm.

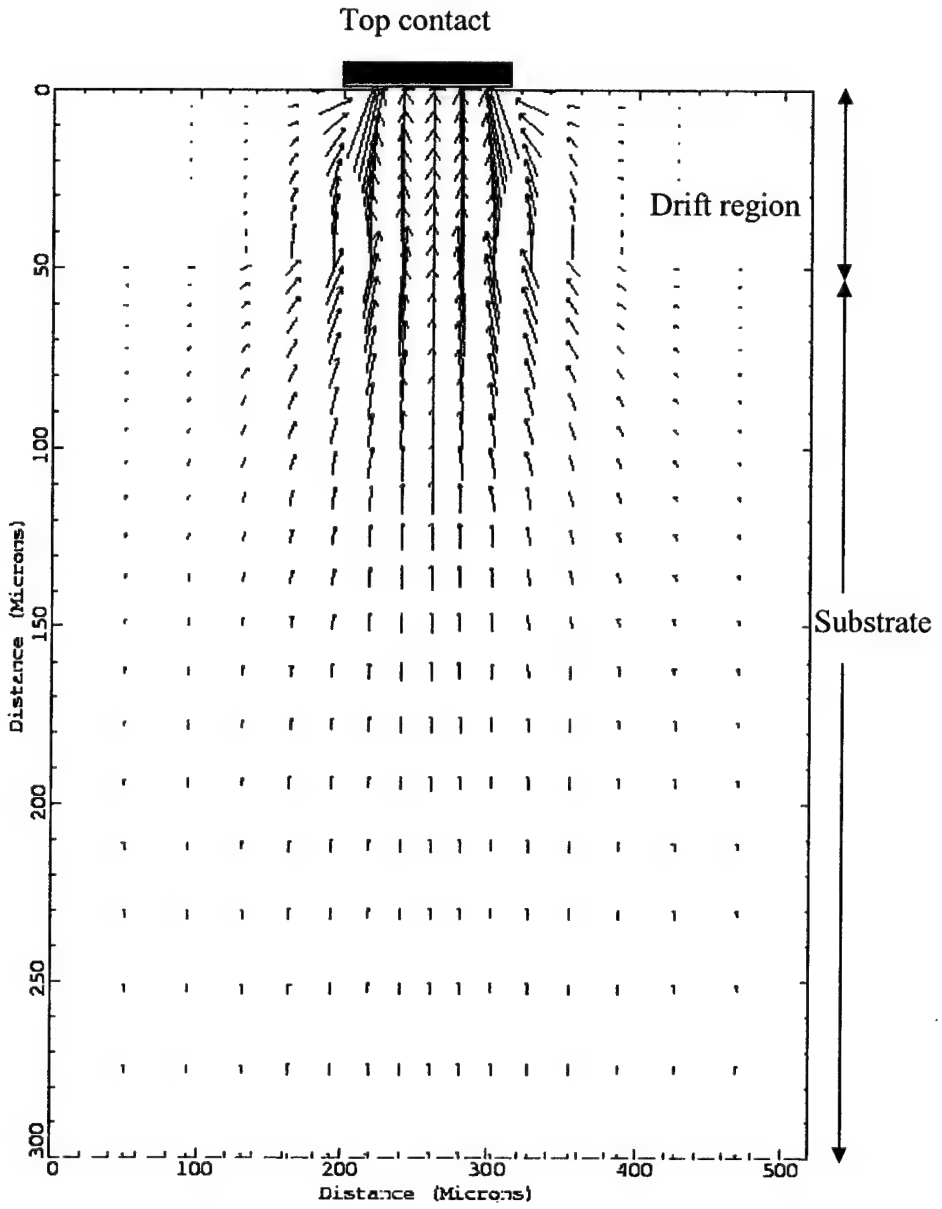


Fig. 8.32. Current flow vectors showing current spreading in the drift region. The top contact area equals to the area for a device with 2-3 design rules and L_{JFET}=8μm. The epilayer doping is $9 \cdot 10^{14}$ cm^{-3} and thickness is 50μm.

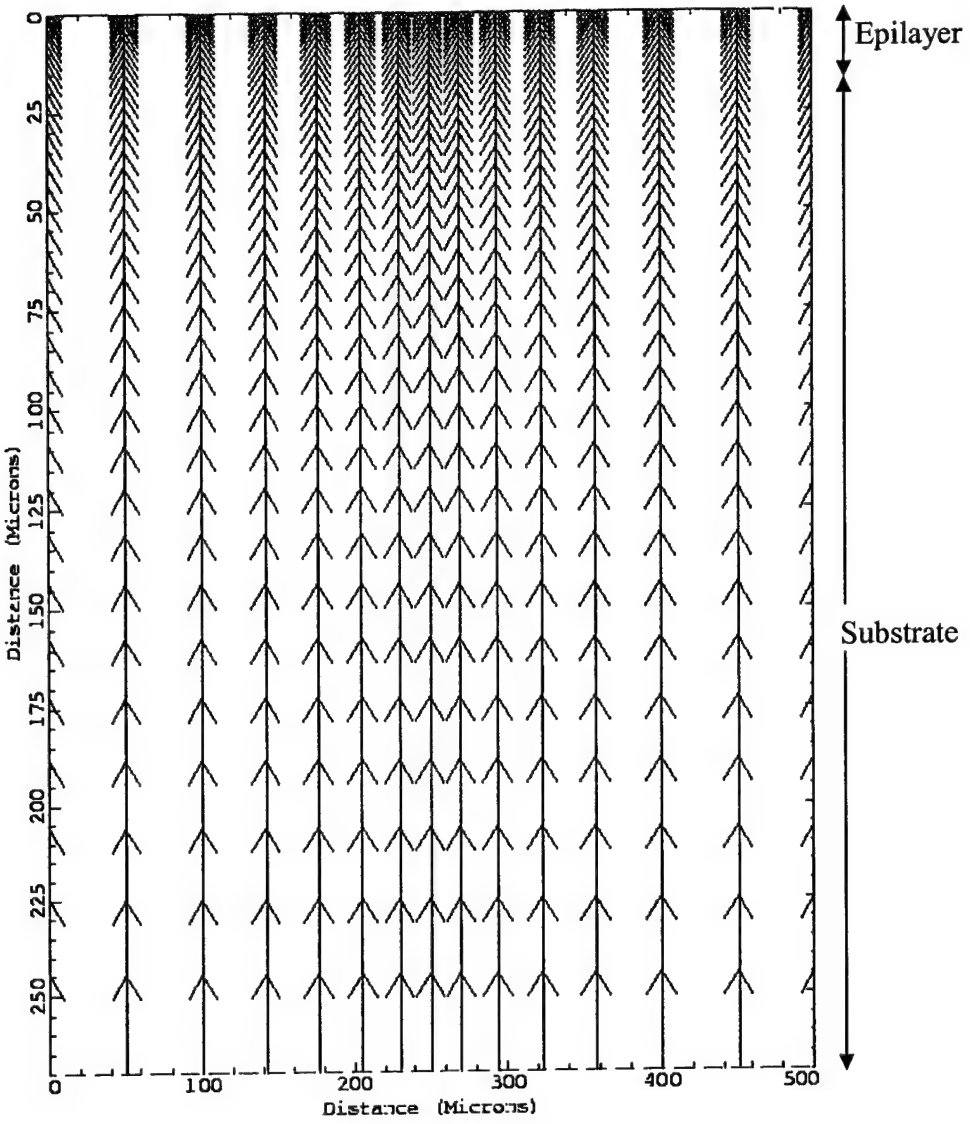


Fig. 8.33. Current flow vectors showing no current spreading. The top contact area equals to the bottom contact area for a device with epilayer doping $3.2 \cdot 10^{15}$ cm^{-3} and thickness 20 μm.

Table 8.2 summarizes the results obtained from the simulations. The corrected Ron,sp is then calculated using the equation 8.10.

$$R_{on,sp,corrct.} = R_{on,sp,meas}. - R_{drift,sp,spreading} + R_{drift,sp,wospreading} \tag{8.10}$$

The $R_{drift,sp,wospreading}$ found from the simulation for a drift doping of $3.2 \cdot 10^{15}$ cm^{-3} and thickness of 20 μm is 4.5 mΩ-cm^2. For a doping of $9 \cdot 10^{14}$ cm^{-3} and thickness of 50 μm it is found to be 35.2 mΩ-cm^2. The drift region resistance with current spreading is less than the one without spreading, and varies with the area of the device. The corrected $R_{on,sp}$ is always greater than the measured $R_{on,sp}$.

Table 8.2

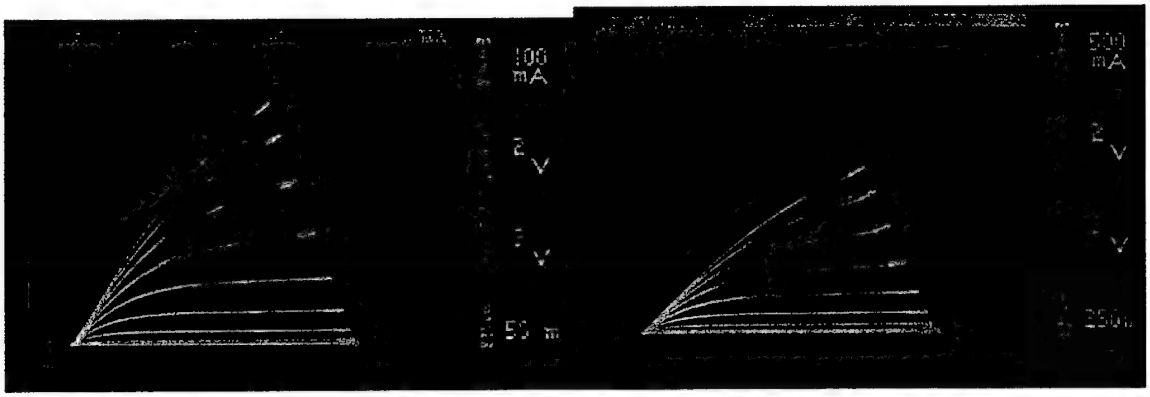
	4H-20μm, N_D=3.2e15 cm^{-3} and T_{epi}=20μm					
	L_{JFET} (μm)	Area x10^{-4} (cm^2)	(Measured) $R_{on,sp,meas}$ (mΩ-cm^2)	(Simulated) With spreading $R_{drift,sp,spreading}$ (mΩ-cm^2)	(Simulated) Without spreading $R_{drift,sp,wospreading}$ (mΩ-cm^2)	Corrected $R_{on,sp,correct}$ (mΩcm^2)
2-3 Design Rules	4	1.04	26.9	2.96	4.5	28.4
	6	1.144	28.0	3.22	4.5	29.2
	8	1.248	26.6	3.78	4.5	27.3
3-5 Design Rules	4	1.456	40.0	2.93	4.5	41.4
	6	1.56	31.8	3.12	4.5	33.1
	8	1.664	36.4	3.09	4.5	37.7
2-3 Design Rules	4H-50μm, N_D=9e14cm^{-3} and T_{epi}=50μm					
	4	1.04	117	17.7	35.2	134.5
	6	1.144	83.1	19.3	35.2	99.0
	8	1.248	74.1	22.4	35.2	86.9

8.7 Large Area Power Devices

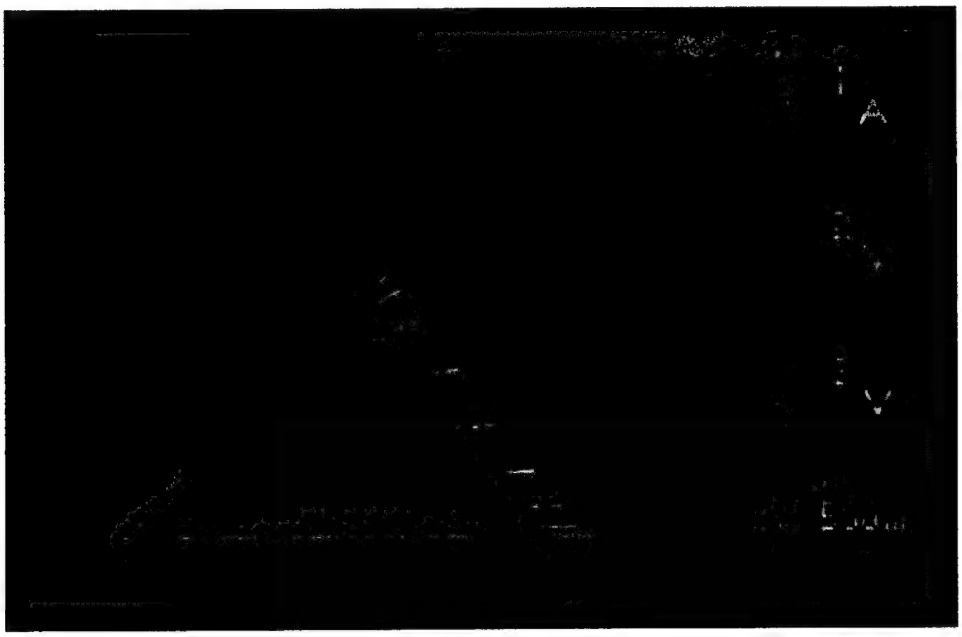
In this process, large area power DMOSFET structures in 0.7mmx0.7mm size with 2-3 and 3-5 design rules, 1.5mmx1.5mm, and 3mmx3mm sizes with 3-5 design rules were fabricated. The ultimate goal is to produce high voltage and high on-current power DMOSFET structures on 4H-SiC material. The forward I-V characteristics were measured with a Tektronix Type576 curve tracer. Figure 8.34a shows the on-state drain characteristics of a 0.7mmx0.7mm DMOSFET with 2-3 design rules, L_{JFET}=6μm, and channel length of 0.5μm on the 4H-20μm. The device active area is $2.844x10^{-3}$ cm^2. The specific on-resistance calculated was 37.9mΩ-cm^2. Figure 8.34b is the I-V characteristics of a 1.5mmx1.5mm device with 3-5 design rules, L_{JFET}=6μm, and active area of $1.25x10^{-2}cm^2$. The specific on-resistance calculated was 54.7 mΩ-cm^2. Figure 8.34c shows the I-V characteristics of a 3mmx3mm device with 3-5 design rules, L_{JFET}=6μm, active area of 0.07515cm^2 and specific on-resistance of 125.2 mΩ-cm^2. The on-resistance increases with device area and cell pitch. With a smaller cell pitch it is possible to obtain much lower on-resistance values from these large area devices.

Power MOSFETs on the 4H-20μm sample showed larger current densities and lower specific on-resistances compared to the 4H-50μm sample. Measurements on the small area power devices on the 4H-50μm sample showed on-resistances of 86.9, 99.0 and 134.5 mΩ-cm^2 for 2-3 design rules and L_{JFET}=8μm, 6μm, and 4μm respectively. The doping of the epilayer is $9 \cdot 10^{14}$ cm^{-3} and thickness is 50 μm, and therefore the drift and JFET resistances will be the dominant resistance contributors to the total on-resistance, and the lowest value of $R_{on,sp}$ can be obtained with a L_{JFET}=8μm and with 2-3 design rules. In 1.5mmx1.5mm and 3mmx3mm devices, 3-5 design rules will increase the specific on-resistance due to larger cell pitch and JFET resistances. Moreover, the source specific on-resistance on this sample was extremely high and this will also increase the $R_{on,sp}$. Figure 8.35a shows the I-V characteristics of a 0.7mmx0.7mm device on a 50 μm epilayer with 2-3 design rules and L_{JFET}=6μm. Figures 8.35b and c show photographs of a 0.7mmx0.7mm device. The specific on-resistance calculated was 170.64mΩ-cm^2. Figures 8.36a and c show the I-V characteristics of a 1.5mmx1.5mm and a 3mmx3mm

device. The specific on-resistances calculated were 156 $m\Omega$-cm^2 and 0.75 Ω-cm^2 respectively. Figures 8.36b and d show respective device photographs.

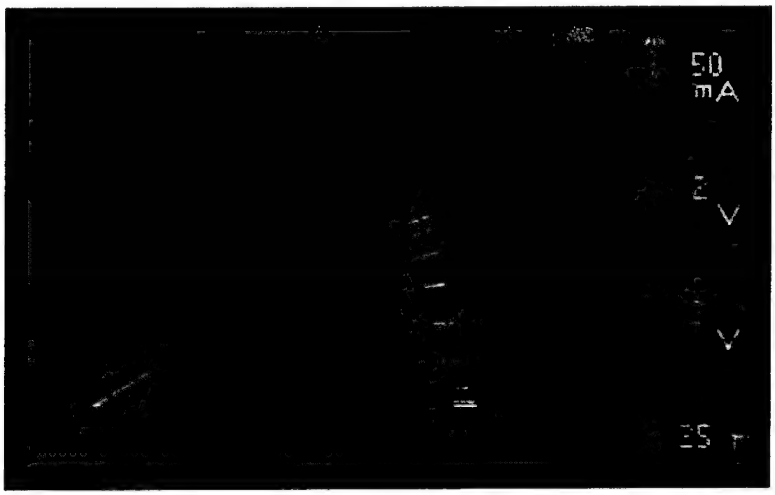


a) 0.7mmx0.7mm device (b132) b) 1.5mmx1.5mm device (b263)

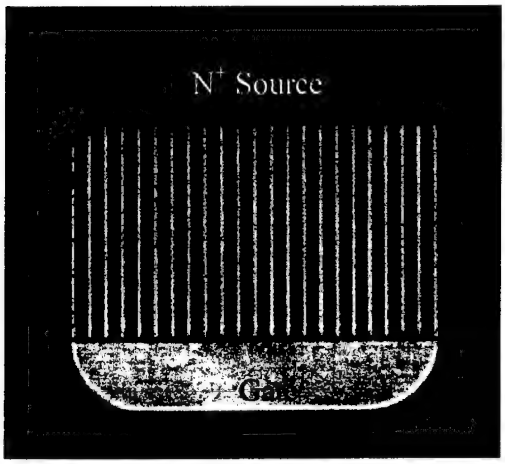


b) 3mmx3mm device (9)

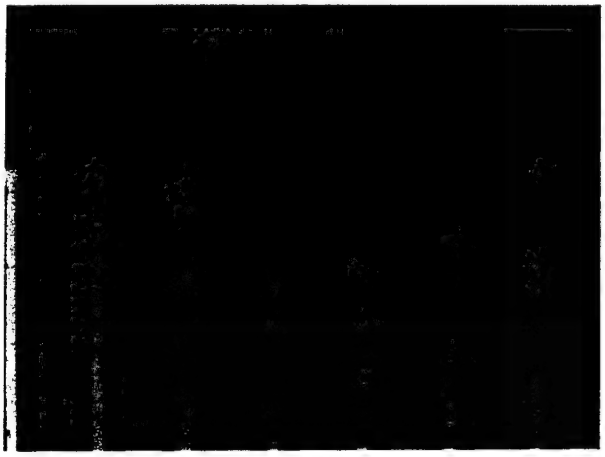
Fig. 8.34. Performance of 0.7mmx0.7mm, 1.5mmx1.5mm, and 3mmx3mm devices on the 4H-20 μm sample with active areas of $2.844x10^{-3}$ cm^2, $0.0125cm^2$, and $0.07515cm^2$ respectively. The maximum gate voltage applied was 20V at 2V step.



a) I-V characteristics. Maximum gate voltage applied was 18V at 2V steps.

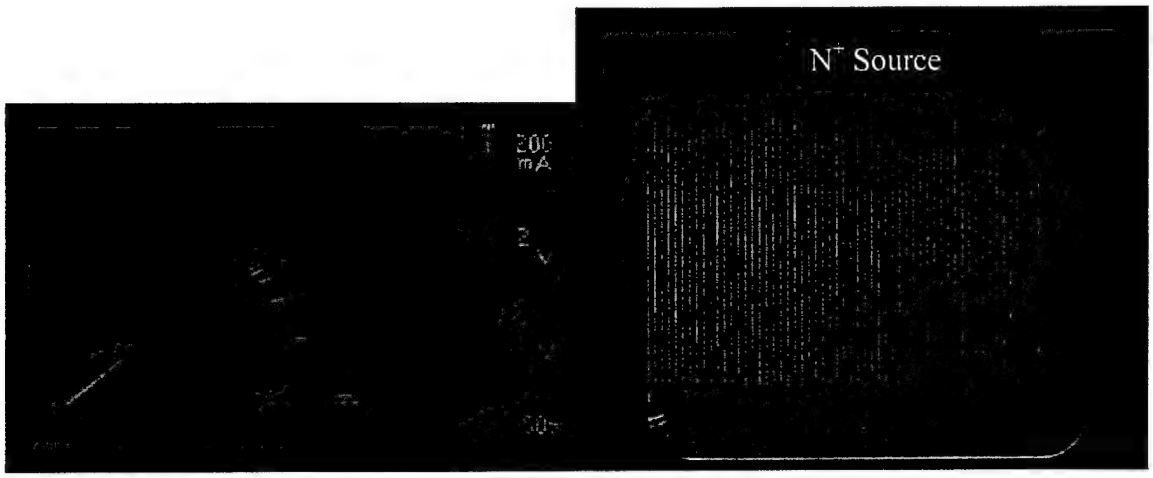


b) 0.7mmx0.7mm device
Magnification x50



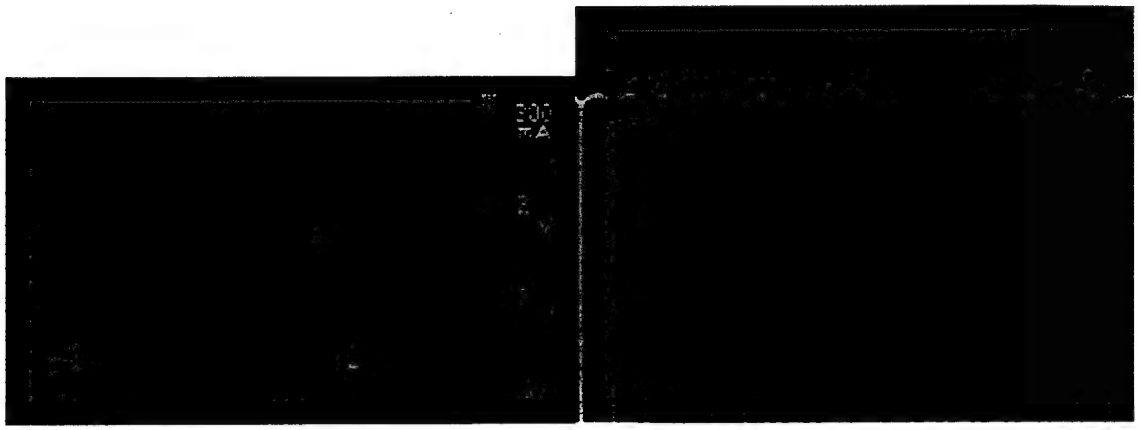
c) 0.7mmx0.7mm device, magnification x500.

Fig. 8.35. Performance of a 0.7mmx0.7mm device on the 4H-50μm sample with active area of $2.844 \times 10^{-3} cm^2$. a) I-V characteristics, and b) and c) device photographs.



a) I-V characteristics of 1.5mmx1.5mm device.

b) 1.5mmx1.5mm device. Magnification x50



c) I-V characteristics of 3mmx3mm device.

b) 3mmx3mm device. Magnification x500

Fig. 8.36. Performance of a 1.5mmx1.5mm and 3mmx3mm device on the 4H-50μm sample with active areas of 0.0125cm^2 and 0.07515cm^2 respectively. a) I-V characteristics, and b) device photograph of the 1.5mmx1.5mm device; c) I-V characteristics, and d) device photograph of the 3mmx3mm device. The maximum gate voltage applied was 18V at 2V steps. Both devices are limited by the JFET and source specific on-resistances.

In conclusion, we have successfully reduced the channel length of a 4H-SiC DMOS structure. The inversion channel resistance is no longer the dominant resistance. However, the source and the JFET resistances now dominate and need to be improved. We have seen that even with perfect alignment, the source resistance may become the dominant resistance and any misalignment makes it worse. The specific on-resistance for a device (m216b) with 2-3 design rules and JFET length of 8μm on the 4H-20μm sample was 27.3 $m\Omega\text{-}cm^2$ (after making corrections for the spreading resistance). This device showed a blocking voltage of 1800V at a leakage current of 0.03mA (see Fig. 8.3). Another device (m2211) on the same sample having 3-5 design rules and JFET length of 6μm, showed a specific on-resistance of 33 $m\Omega\text{-}cm^2$ (corrected) and blocking voltage of 2000V at a leakage current of 0.2μA (see Fig. 8.5). On the 4H-50μm sample, a device (m1265) having 2-3 design rules and a JFET length of 8μm showed a specific on-resistance of 87 $m\Omega\text{-}cm^2$ (corrected). However, the maximum blocking voltage capability of devices on the 4H-50μm sample were reduced to ~2kV, which is probably process related, as earlier we achieved 4.5kV blocking from a diode. The specific on-resistance is not as low as expected. We have eliminated the inversion channel resistance, but $R_{source,sp}$ and $R_{accu,sp}$ have become very important. To decrease the $R_{source,sp}$ the contact resistivity needs to be improved. Different designs need to be studied and employed so that the source resistances become less sensitive to misalignments. A low kV device design with higher drift region doping would have an advantage, since the accumulation channel mobility would be higher and the threshold voltage V_{TD} more negative due to the higher doping.

9. CONCLUSIONS AND RECOMMENDATIONS FOR FUTURE WORK

This thesis focuses on the design, fabrication, characterization, and development of power DMOS transistors in 4H-SiC material. 4H-SiC material shows significant promise for high-temperature, high-voltage power device applications due to its large bandgap, high critical electric field, and high relatively isotropic electron mobility. However, 4H-SiC DMOSFETs suffer from low inversion channel mobility in the implanted p-well regions. The goal of this work was to lower the inversion channel resistance of the DMOS transistors. The following list summarizes the work performed in developing the 4H-SiC DMOS transistors:

1. Investigated three different device structures, namely the "etched epitaxial base DMOSFET" (epiDMOS and epiAFET), the "implanted epitaxial base DMOSFET", and the all implanted "short-channel counter-doped self-aligned DMOSFET".

2. Simulated the epiDMOS, epiAFET, and the implanted epitaxial base DMOS structures and showed that the specific on-resistance in these devices is physically limited due to alignment problems and the requirement of a high cell pitch. Fabricated epiDMOS structures showed high on-resistances. In addition to the n-plug being resistive, this structure was difficult to fabricate as it required an epigrowth over an etched surface which resulted in a "tapered epi" problem and consequently resulted in the discontinuity of the channel.

3. Designed and developed a novel self-aligned short-channel DMOS structure, which allowed successful fabrication of $L_{ch} \leq 0.5\mu m$ and significantly reduced the inversion channel resistance.

4. Developed an improved method of introducing counter-doped implants to improve MOS inversion channel mobility, lower threshold voltage, and reduce the stress on the gate dielectric without lowering the blocking voltage.

5. Developed a self-aligned source and base contact process to reduce the cell pitch and thereby reduce the specific on-resistance.

6. Activated the p-type implantations in a silane ambient to improve inversion channel mobility by minimizing the step bunching phenomenon.

7. Incorporated the counter-doped channel and the NO post-oxidation anneal to improve inversion channel mobility.

8. Implemented the JTE technology to improve the blocking voltage capability.

In this work, we have successfully demonstrated a 4H-SiC self-aligned short-channel counter-doped DMOS structure which is not dominated by the inversion channel resistance. However, the source and accumulation channel resistances have become the dominant resistance components. The source specific on-resistance was found to dominate even with perfect alignments due to high contact resistances. As the device is scaled down, any misalignment of the masks during contact formation can increase the source resistance drastically. The specific on-resistance is not as low as expected. The accumulation channel resistance does not get reduced by the counter-doped implants, since they are restricted to the channel region.

To reduce the source resistance, the contact formation process needs to be improved. In the future, by letting the source contact to run up to or go over the oxidized poly gate we can avoid misalignment problems for the source contact as shown in Fig. 9.1. However, we still need to worry about the misalignments of the p^+ contact, the oxide window etch, and the p^+ implants.

The accumulation channel resistance can be lowered by increasing the accumulation channel mobility or by making V_{TD} more negative. It can also be lowered by making the JFET gap smaller. This also reduces the cell pitch. However, for high kV designs where the drift region doping is low, this scaling will be limited by the JFET resistance. To prevent the JFET pinching, a heavily doped deep JFET spacer implant can

be performed, as shown in Fig. 9.1 [71]. This will allow the JFET length to be smaller, lower the JFET resistance, and avoid high field stress in the oxide.

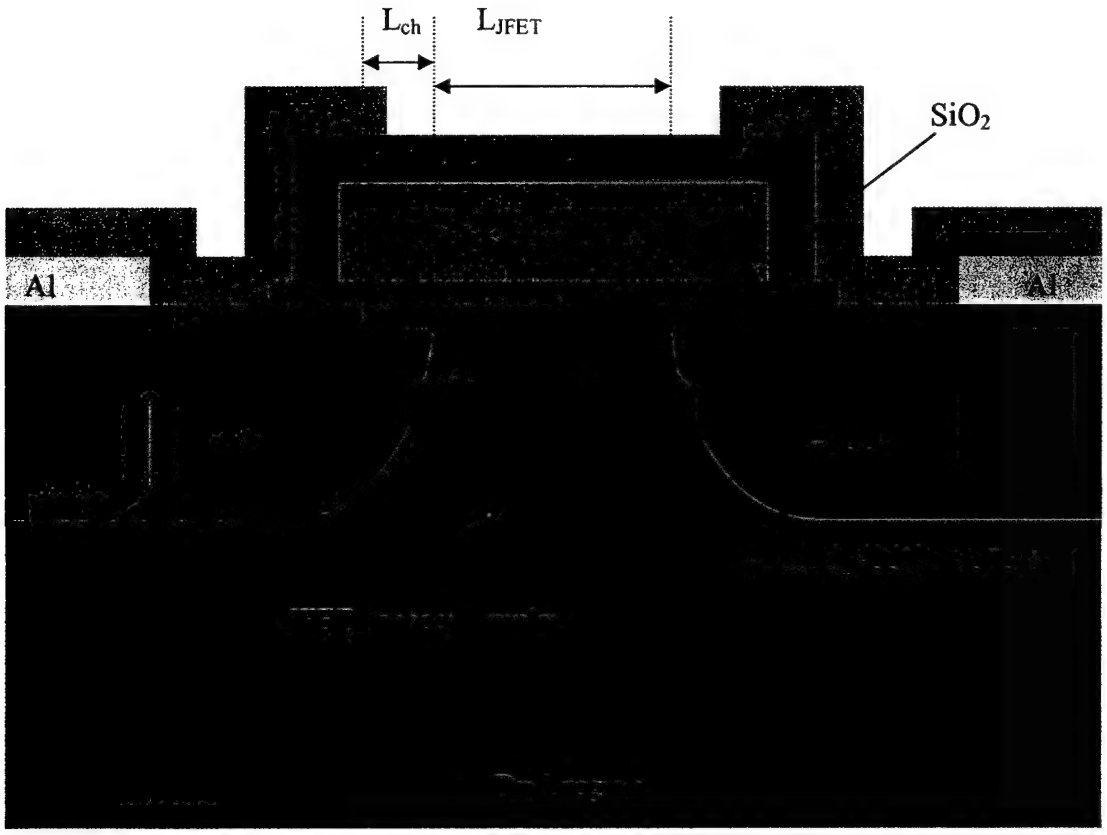


Fig. 9.1. Schematic cross-section of the suggested DMOS structure.

Another way of reducing the accumulation channel resistance is to switch to a low kV design. A low kV design with a high drift region doping serves as an advantage as the V_{TD} is more negative. From simulations we find that the short-channel structure is particularly suitable for the 600 to 1200V range, where the specific on-resistance can be lowered by 4 to 6 times by decreasing the channel length from 3 to 0.5μm. In the future, the process developed in this thesis can be used to fabricate short-channel MOSFETs on a 6μm epilayer with 2e16 cm^{-3} doping (1kV design) to achieve a $R_{on,sp}$ less than 10 mΩ-cm^2.

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